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Modules

Product Technical Specification

RC71xx

May 2024

41114670 Rev. 3.1

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Sierra Wireless

Semtech Corporation acquired Sierra Wireless in January 2023. The Sierra Wireless brand is gradually being phased out. During the phase-out period, references to both “Semtech” and “Sierra Wireless” may appear in product documentation.

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Revision History

Revision number	Release date	Changes
1	May 2023	Creation
2	December 2023	Added Product Features Updated Table 1-5: Module Dimensions (module weight) Updated Table 3-1: Environmental Specifications (ambient operating temperature) Updated Table 3-3: Operating Conditions (output current rating) Added Under-Voltage Lockout (UVLO) Updated Table 3-5: Power States (Lite Hibernate / Hibernate descriptions) Updated Power Consumption States Updated Table 3-7: Modem Wakeup Sources (Software) (added footnote) Updated Table 3-8: Modem Wakeup Sources (Hardware) (added footnotes) Updated Table 3-11: RC7110 Current Consumption Values Updated Table 3-12: RC7120 Current Consumption Values Updated Table 3-16: RC7110 Conducted Rx Sensitivity—LTE Bands Updated Table 3-17: RC7120 Conducted Rx Sensitivity—LTE Bands Updated Table 3-19: Antenna Recommendations (MEG) Updated Table 3-20: Absolute Maximum Ratings (TJ) Updated Power Consumption States Added Power-up Sequence Added Software-Initiated Power Down Removed 4.2 Emergency Power Off Added USB (added note) Updated Table 4-7: UIM1 Interface Pins (UIM1_DATA footnote) Updated Table 4-8: External UIM2 Interface (UIM1_DATA footnote) Updated GPIO details / references: Digital I/O Characteristics; Table 4-9: GPIO Pin Description (Continued on next page)

Revision number	Release date	Changes
		(Revision 2 changes continued from previous page) Updated Table 4-11: VGPIO Electrical Characteristics (current capability) Updated VGPIO (updated note) Updated Table 4-13: Reset Timing Updated Table 4-15: ADC Interface Characteristics Updated TP1 (Boot Pin) Updated Table 4-17: Recommended Test Points (updated TP1) Updated Figure 4-5: Recommended WWAN_LED_N Connection (resistor detail) Updated Table 4-20: UART1_RI (Ring Indicator) Timing Parameters (updated TP1) Added SAFE_PWR_REMOVE Added Specific Design Rules to Support TRP Performance Added Specific Design Rules to Support TIS Performance Added Thermal Considerations Replaced Reliability Specification Updated Table 9-1: Pin Definitions voltage / pull type / function (UART1_RI, UART1_DTR, UART1_DSR, GPIO2, USB_VBUS, UIM2_RESET_N, POWER_ON_N, GPIO4, GPIO42, GPIO2, SAFE_PWR_REMOVE) Updated Table 9-2: RF Pin Information (USB_VBUS) Updated Packaging Added Testing
3	May 2024	Updated Interfaces: VPIO description Updated chapter 3 Environmental (temperature classes) Updated Table 3-11: RC7110 Current Consumption Values & Table 3-12: RC7120 Current Consumption Values: Added Sleep2 USB OFF explanatory footnote Reformatted Table 3-13: Supported LTE Bands Added Table 3-21: Digital Interface Characteristics — Summary Updated Table 3-22: Digital I/O Characteristics — VDD_IO = 1.80 V (nominal): Clarified footnote on table applicability to interfaces; Added footnote for effect of IO_VOL_SEL pin. Added Table 3-23: Digital I/O Characteristics — VDD_IO = 3.30 V (nominal) for 3.3 V input characteristics Updated Table 3-24: Digital Output Characteristics — VDD_IO = 1.80 V (nominal): Changed title for consistency Updated Table 3-25: Digital Input Characteristics — VDD_IO = 1.80 V (nominal): Clarified footnote on table applicability to interfaces; Updated section POWER_ON_N: Added Important power down note Updated Table 4-2: POWER_ON_N Timing Parameters: Updated timing parameter values Updated section UART: Clarified description Updated Table 4-8: External UIM2 Interface: Updated footnote for effect of IO_VOL_SEL pin. Updated section VGPIO: Added 3.3V content Updated Table 4-19: LED Interface Pin: Added 3.3V content Updated Table 4-22: SAFE_PWR_REMOVE Timing Parameters: Updated SAFE_PWR_REMOVE timing parameter value. Updated Figure 4-8: SAFE_PWR_REMOVE: Updated SAFE_PWR_REMOVE timing parameter value. (Continued on next page)

Revision number	Release date	Changes
		(Revision 3 changes continued from previous page) Updated W_DISABLE_N — Wireless Disable: Added 3.3V VGPIO content. Updated Power Supply: Updated recommended trace width. Updated Figure 5-8: Recommended UIM Holder Implementation for UIM1 and UIM2: Updated capacitors on UIM_VCC Updated chapter Regulatory Compliance and Industry Certifications: Changed title; reorganized topics; reformatted Table 8-2 Updated Table 9-1: Pin Definitions: Updated pin details for pins 2–10, 40, 41, 45–47, 96–99, 106, 109, 110, 144–152, 155, 156, 159 Added appendix References
3.1	May 2024	Updated Environmental (corrected labels for Class A and Class B temperature descriptions)

Contents

1: About This Document

This document defines the high-level product features and illustrates the interfaces for the Sierra Wireless RC71xx Embedded Modules. It covers the hardware aspects of the product series, including electrical and mechanical.

Note: Sierra Wireless modules are shipped factory-programmed, with industry or mobile operator approved firmware, according to the specific SKU ordered. Periodically, newer firmware versions become available and can include new features, bug fixes, or critical security updates. Sierra Wireless strongly recommends that customers establish their own production capability for updating module firmware on their assembled end platform, in the event that a newer firmware must be installed before deployment.

1.1 General Features

The Sierra Wireless RC71xx is an industrial-grade LGA 239-pad embedded module. Its wireless modem provides data connectivity on the networks listed in Table 1-1.

Table 1-1: Supported Networks and Voice Capability

Variant	Network	Network Voice Support	LTE Category
RC7110	LTE	NA (Data only)	Cat 1bis
RC7120			

Table 1-2 and Table 1-3 detail supported RF bands / connectivity.

Table 1-2: RC7110 Supported Bands / Connectivity

Technology	RF Band	Transmit Band (Tx) (MHz)	Receive Band (Rx) (MHz)	Notes
LTE	B2	1850–1910	1930–1990	
	B4	1710–1755	2110–2155	
	B8	880–915	925–960	
	B12	699–716	729–746	
	B13	777–787	746–756	
	B66	1710–1780	2110-2200	

Table 1-3: RC7120 Supported Bands/Connectivity

Technology	RF Band	Transmit Band (Tx) (MHz)	Receive Band (Rx) (MHz)	Notes
LTE	B1	1920–1980	2110–2170	
	B3	1710–1785	1805–1880	
	B7	2500–2570	2620–2690	
	B8	880–915	925–960	
	B20	832–862	791–821	
	B28	703–748	758–803	

1.2 Product Features

Table 1-4 provides an overview of the Sierra Wireless RC71xx module's product features:

Table 1-4: Product Features

Feature	Description
Chipset design	▪ Up to 204 MHz built on Arm Cortex-M3 technology ▪ 4 MB NOR flash for AP, 1 MB NOR flash for CP
Power Manager Unit	▪ Ultra-low power consumption operation — PSM, and eDRX ▪ Six external wakeup sources ▪ Supports LPUART(Low Power UART) to receive UART messages from host while in Sleep power state ▪ AON (Always ON) Watchdog
RF	▪ Supports Power Class 3 ▪ Supports 1T1R and supports Full duplex ▪ Supports RFFE time-accurate GPIOs to drive various PA+ASM
Operating system	▪ FreeRTOS, base ARM CMSIS-RTOS version 2
Security	▪ System Security — Secure boot ▪ Hardware encryption and decryption ▪ Flash encryption ▪ True random number generator ▪ Network Security: ▪ DTLS, SSL 3.0, TLS 1.2 ▪ AES, 3DES, DES, ARC4 ▪ MD5, SHA-1, SHA-256 ▪ RSA/PKCS #1 v1.5
System update	▪ Delta FOTA
Network Protocol	▪ IPv4/v6 (LWIP) ▪ Networking protocols: ▪ TCP, UDP, HTTP(S), FTP ▪ IOT CoAP and MQTT client 3.1.1

Table 1-4: Product Features (Continued)

Feature	Description
Host Network interface	▪ USB 2.0 — RNDIS (Win and Linux), ECM (Linux and Mac), or PPP ▪ UART — PPP
Appication interface	▪ AT commands: · Basic commands are compliant with ITU-T V.250 · 3GPP TS 27.007 v16.0.0 · 3GPP TS 27.005 v15.0.0 · Proprietary extended AT commands ▪ Command interfaces — USB, or UART

1.3 Interfaces

The Sierra Wireless RC71xx provides the following interfaces and peripheral connectivity:

- UIM interface — See UIM Interface
- VBAT_RF/VBAT_BB power supply — See Power Supply Ratings
- RF — See RF
- ON/OFF control:
  - POWER_ON_N — See POWER_ON_N
  - Reset signals — See Reset Signals (RESET_IN_N and RESET_OUT_N)
- USB 2.0 — See USB
- UART serial links — See UART
- GPIOs — See General Purpose Input/Output
- 1.8V /3.3V voltage reference — See VGPIO
- ADCs — See ADC
- Antenna control — See Antenna Control
- Test pins — See Test Points

1.4 Common Flexible Form Factor (CF3)

The Sierra Wireless RC71xx belongs to the Common Flexible Form Factor (CF3) family of WWAN modules. These modules share the same mechanical dimensions (same width and length with varying thicknesses) and footprint. The CF3 form factor provides a unique solution to a series of problems faced commonly in the WWAN module space as it:

- Accommodates multiple radio technologies and band groupings
- Supports bit-pipe (Essential Module Series) and value-add (Smart Module Series) solutions
- Offers electrical and functional compatibility

1.5 Physical Dimensions and Connection Interface

The Sierra Wireless RC71xx module is a compact, robust, fully shielded and labeled (laser-etched) module with the dimensions noted in Table 1-5.

Table 1-5: Module Dimensions[a]

Parameter	Nominal	Tolerance	Units
Length	23.00	±0.10	mm
Width	22.00	±0.10	mm
Thickness	2.50	±0.20	mm
Weight	2.3	±0.2	g

a. Dimensions are accurate as of the release date of this document.

The Sierra Wireless RC71xx module is an LGA form factor device. All electrical and mechanical connections are made through the 238 Land Grid Array (LGA) pads and 1 polarity mark on the bottom side of the PCB. (See Figure 1-1 for details.)

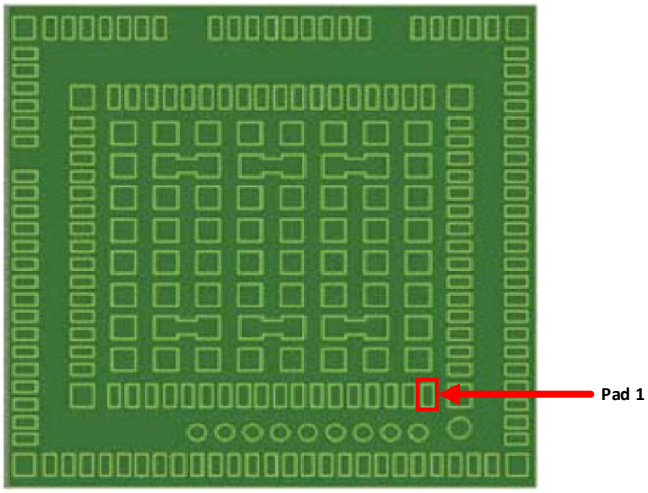


Figure 1-1: RC71xx Series Module Bottom View

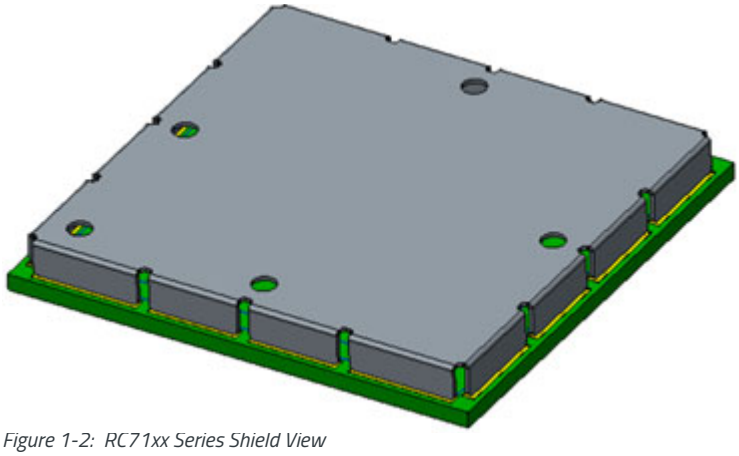


Figure 1-2: RC71xx Series Shield View

The 239 pads have the following distribution:

Table 1-6: LGA Pad Types

Pad Type / Quantity		Dimensions	Pitch
Signal Pads	66 inner pads	1.0x0.5 mm	0.8 mm
	91 outer pads		
Test Points	9 test points	0.8 mm (diameter)	1.20 mm
Ground Pads	64 inner pads	1.0x1.0 mm	1.83 mm / 1.48 mm
	4 inner corner pads	1.0x1.0 mm	–
	4 outer corner pads	1.0x0.9 mm	–
Polarity Mark	1 polarity mark (Ground)	1.0 mm (diameter)	–

2: Functional Specifications

2.1 Architecture

The following figure presents an overview of the Sierra Wireless RC71xx module's internal architecture and external interfaces.

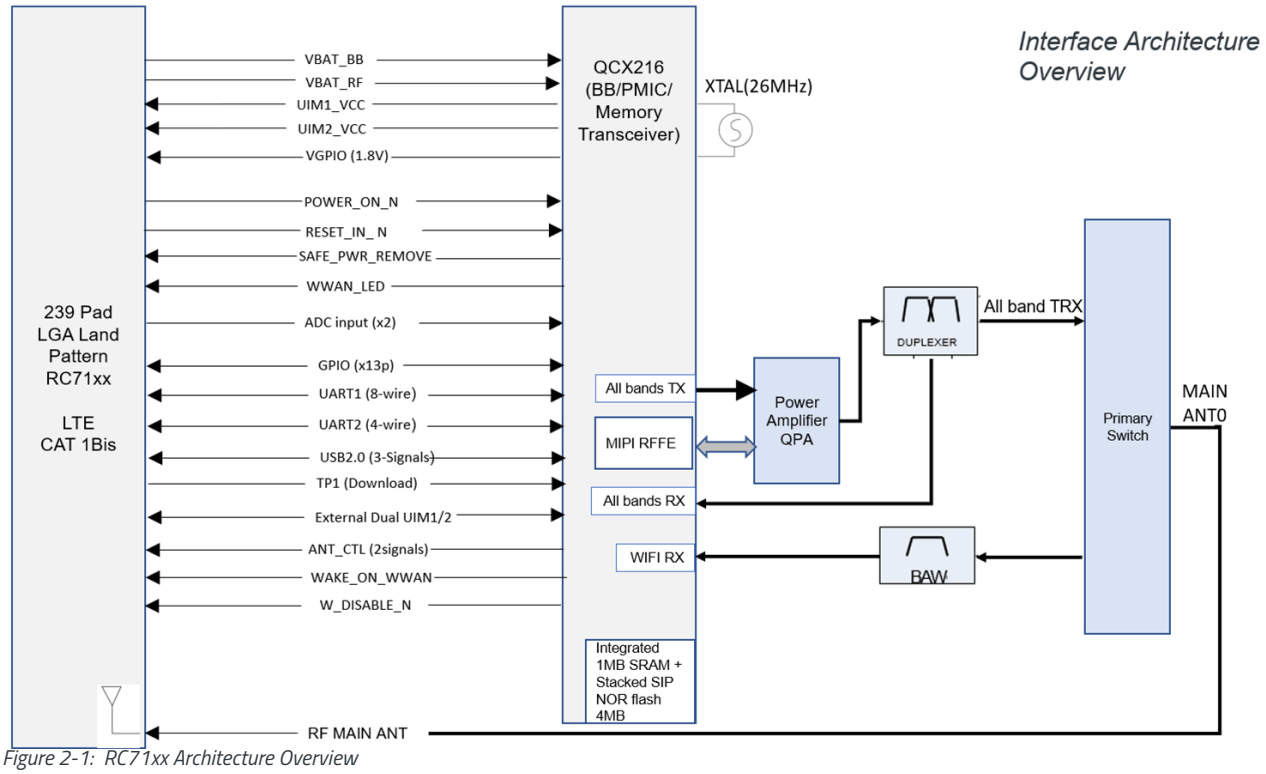


Figure 2-1: RC71xx Architecture Overview

2.2 Telecom Features

Table 2-1 summarizes the Sierra Wireless RC71xx module's capabilities offered through the Telecom core.

Table 2-1: Module Capabilities

Feature	Description
Electrical	3.4–4.3V supply voltage (VBAT_BB, VBAT_RF): ▪ Single supply, VBAT_BB tied to VBAT_RF *or* ▪ Dual supplies, single supply each for VBAT_BB and VBAT_RF

Table 2-1: Module Capabilities (Continued)

Feature	Description
SMS	▪ SMS MO and MT ▪ SMS over SGs support ▪ SMS saving to UIM card or ME storage ▪ SMS reading from UIM card or ME storage ▪ SMS concatenation ▪ SMS Status Report ▪ SMS storing rules (support of **AT+CNMI**, **AT+CNMA**)

2.2.1 Network Technology Specifications

2.2.1.1 LTE Specifications

The following table describes LTE specifications for Sierra Wireless RC71xx modules.

Table 2-2: Supported LTE Specifications

Standard	Feature Description
3GPP R14	▪ eDRX (Extended Discontinuous Reception) to extend battery life in devices that do not require frequent network access ▪ PSM (Power Saving Mode) to reduce power consumption ▪ Data rates: Cat 1bis FDD (up to 10 Mbps downlink, 5 Mbps uplink)
System Determination	▪ Frequency Scan and System Selection within LTE ▪ LTE BPLMN support ▪ Standalone Security, Dedicated EPS Bearer Management and Dormancy ▪ Carrier Specific BSR Requirements
Data	▪ Multiple cellular packet data profiles ▪ Mobile-originated PDP context activation/deactivation ▪ PDP context type (IPv4, IPv6, IPv4v6) ▪ RFC1144 TCP/IP header compression

3: Technical Specifications

3.1 Environmental

The environmental specifications for operation and storage of the Sierra Wireless RC71xx are defined in Table 3-1.

Table 3-1: Environmental Specifications

Parameter	Range	Description
Ambient Operating Temperature	-30°C to +70°C	Class A (3GPP compliant)
	-40°C to +85°C	Class B (Operational, non-3GPP compliant), reduced operating parameters required)
Ambient Storage Temperature	-40°C to +85°C	–
Ambient Humidity	85% or less	–

Important: *The internal chipset temperature (reported by AT!PCTEMP?) must be kept below 92 °C, and the internal PA temperature (reported by AT!PATEMP?) should be kept below 85 °C.*

Class A is defined as the operating temperature range within which the device:
- Shall exhibit normal function during and after environmental exposure.
- Shall meet the minimum requirements of 3GPP or appropriate wireless standards.

Class B is defined as the operating temperature range within which the device:
- Shall remain functional during and after environmental exposure
- Shall exhibit the ability to establish any of the device's supported call modes (SMS, Data) even when one or more environmental constraints exceed the specified tolerance.
- Unless otherwise stated, full performance should return to normal after the excessive constraint(s) have been removed.

3.2 Power Supply Ratings

The Sierra Wireless RC71xx operates using DC power supplied via the VBAT_RF and VBAT_BB signals. Power supply options are:
- A single regulated DC power supply (3.7 V nominal)
- Two regulated DC power supplies (3.7 V nominal), one each for VBAT_BB and VBAT_RF

Table 3-2: Power Supply Pins

Pin	Name	Direction	Function	Notes
63, 158	VBAT_BB	Input	Baseband power supply	63 — Must be used 158 — Optional
61, 62, 157	VBAT_RF	Input	RF power supply	61/62 — Must be used 157 — Optional

Table 3-3: Operating Conditions

Parameter		Min	Typ	Max	Units	Notes
Power supply voltage[a,b]		3.4	3.7	4.3	V	Must be within min/max values over all operating conditions (including voltage ripple, drop, and transient).
Power supply ripple		–	–	100	mV_{pp}	See Figure 3-1.
Power supply voltage drop		–	–	250	mV_{pp}	See Figure 3-1 and Figure 3-2.
Power supply voltage transient (overshoot/undershoot)		–	–	300	mV_{pp}	See Figure 3-1.
Output current rating[c]	LTE	–	750	–	mA	▪ Typical value varies and depends on output power, band, and operating voltage. See Current Consumption for values measured under normal operating conditions. ▪ Max value measured over 100 µs period.

a. Power supply voltage outside the required range may affect call quality (dropped calls, data transfer errors, etc.)
b. For Absolute Maximum Ratings, see Table 3-20.
c. These values include a margin. For information on current consumption, see Current Consumption.

Customer should characterize the ripple, drop, and transient response (overshoot/undershoot) of the power supply delivery system at the module input under full transmit power in Sierra Wireless RC71xx modules. To minimize voltage variation, add suitable capacitors to the supply line as close as possible to the module — depending on the power supply design, these capacitors may range from tens to several thousand µF.

Depending on the quality and stability of the power supply, the capacitance value may need to be adjusted if there is any voltage drop or RF interference caused by power fluctuations during module operation.

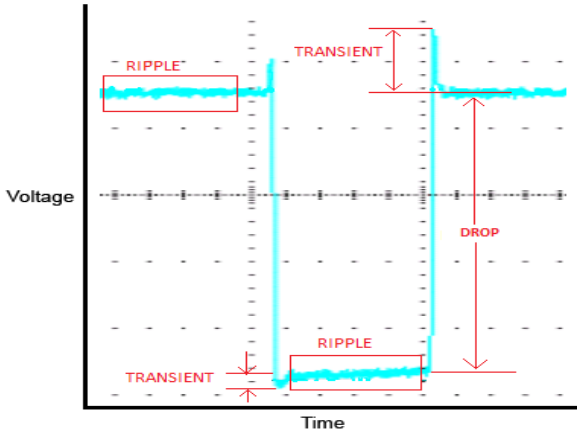


Figure 3-1: Power Supply Characteristics

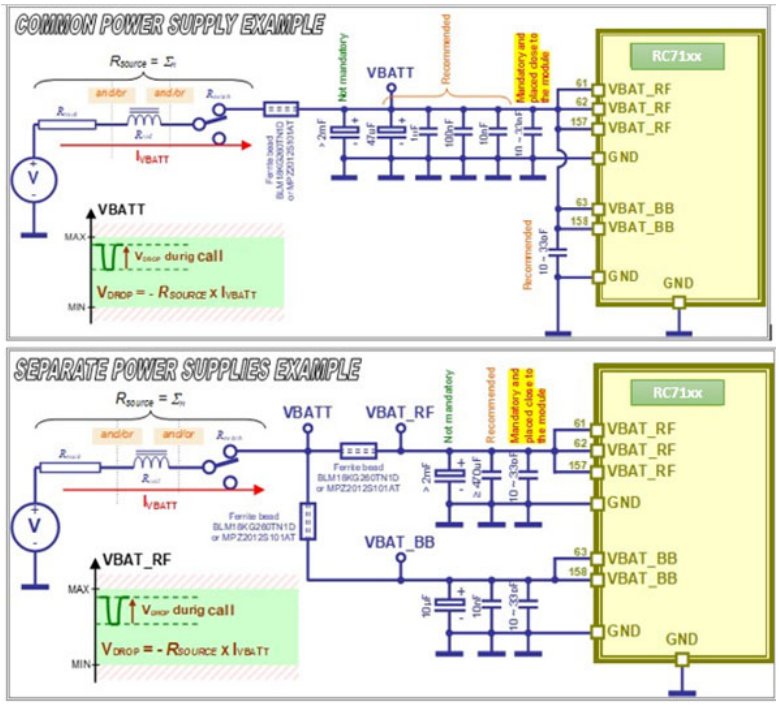


Figure 3-2: Common and Separate Power Supply Examples

3.2.1 Under-Voltage Lockout (UVLO)

The power management section of the Sierra Wireless RC71xx includes an under-voltage lockout circuit that monitors supply and shuts down when VBAT_BB falls below the threshold.

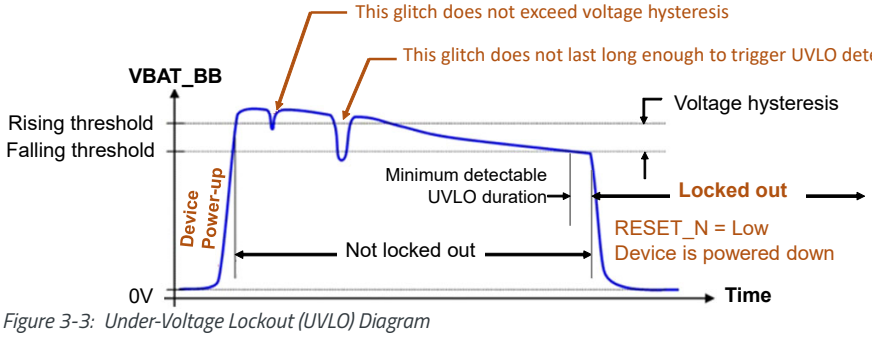


Figure 3-3: Under-Voltage Lockout (UVLO) Diagram

The RC71xx will power down and remain off until VBAT_BB returns to the valid range and the ON/OFF signal is active.

Table 3-4: UVLO Specifications

Parameter	Min	Typ	Max	Units
Threshold voltage, falling	2.0	2.2	2.4	V
Threshold voltage, accuracy	-50	–	+50	mV
Hysteresis	–	200	–	mV
UVLO detection interval	–	10	–	µs

Note: Due to the minimum voltage requirement of 3.3V for USB I/O and RF PA power, if the voltage falls below this threshold, both the USB and RF functionalities will be the first to cease functioning.

3.2.2 Sudden Power Loss

Any sudden power loss of the embedded module during operating mode will increase the NVM crash risk, even in the power on or power down sequence. It is strongly recommended to remove the power only after the module is in power down mode.

3.2.3 Power Consumption States

The Sierra Wireless RC71xx has five basic power states as shown in Table 3-5 — Active, Sleep, Lite-Hibernate, Hibernate, and Off. The RC71xx also supports 3GPP power saving features, including Power Saving Mode (PSM) and Extended Discontinuous Reception (eDRX).

Table 3-6 summarizes the effect of the power states on the module's functionality.

Table 3-7 describes power saving features that are used in lower-power states (i.e., not Active/Idle state), and Table 3-8 describes indicates the hardware wakeup sources for the Lite Hibernate and Hibernate power states.

Table 3-5: Power States

Power State	Description
Active/Idle	▪ Highest power consumption state ▪ All OS system interrupts can wakeup task. ▪ Network IP data transmission
Sleep	▪ Lower power consumption than Active/Idle, but higher than Lite Hibernate ▪ No delay for incoming/outgoing data session
Lite Hibernate	▪ Application Processor is OFF, and cellular processor (modem) is possible in DRX or eDRX state. ▪ Retention IO[a] keeps its state (latch level — high or low) when it enters Lite Hibernate.
Hibernate	▪ Application Processor is OFF, and cellular processor (modem) is possible in eDRX or PSM state, or in LPM (Low Power mode). ▪ Retention IO[a] is OFF (it does not keep its state (latch level — high or low) when it enters Hibernate), and module is in lowest power consumption state.
Off	Module is off (VBATT is ON): ▪ Active state (POWER_ON_N is asserted) — This is a low level signal to turn on the module. ▪ POWER_ON_N is deasserted

a. Retention IOs — GPIO2, GPIO21, UART1_RI, UART1_DSR

Table 3-6: Power States — Module Functionality

Power State	AP Proc[a]	SRAM	General I/O	Retention I/O
Active/Idle	Active/Idle	ON	ON	ON
Sleep	Sleep	ON	ON	ON

Table 3-6: Power States — Module Functionality (Continued)

Power State	AP Proc[a]	SRAM	General I/O	Retention I/O
Lite Hibernate	OFF	OFF	OFF	ON
Hibernate	OFF	OFF	OFF	OFF

a. AP Proc — Application processor for FreeRTOS

Table 3-7: Modem Wakeup Sources (Software)

Power Saving Feature	Possible Power States[a]	Wakeup Source
DRX	Sleep, Lite Hibernate	▪ MT SMS ▪ MT IP Data Receiption ▪ Cell Coverage Recovery
eDRX	Sleep, Lite Hibernate, Hibernate	▪ MT SMS ▪ MT IP Data Reception ▪ Cell Coverage Recovery
PSM	Hibernate	▪ T3412 expired (TAU)
Airplane Mode (+CFUN=0)	Hibernate	

a. AT!CUSTOM="SIMPOWERSAVE",1 must be issued to enable the SIM to enter power saving mode when the module is in sleep state. If SIMPOWERSAVE=0, the module will not be able to enter Lite-Hibernate or Hibernate. For details, refer to *[1] RC71xx AT Command Reference (Doc# 41114675)*.

Table 3-8: Modem Wakeup Sources (Hardware)[a]

Wakeup Source	Wakeup Source state
Wakeup pins[b]	
GPIO2	Edge Rising or Falling
GPIO4	Edge Rising or Falling
GPIO21	Edge Rising or Falling
GPIO42	Edge Rising or Falling
UART Functions	
UART_DTR	Edge Falling, Assert Low[c]
UART_TX	UART serial port input character
SIM Functions	
UIM1_DET	Insert Card, Edge Rising Remove Card, Edge Falling
UIM2_DET	Insert Card, Edge Rising Remove Card, Edge Falling
Power pins	
POWER_ON_N	Edge Falling

a. AT!CUSTOM="SIMPOWERSAVE",1 must be issued to enable the SIM to enter power saving mode when the module is in sleep state. If SIMPOWERSAVE=0, the module will not be able to enter Lite-Hibernate or Hibernate. For details, refer to *[1] RC71xx AT Command Reference (Doc# 41114675).*
b. GPIO2, GPIO4, GPIO21 and GPIO42 can be configured as wakeup sources using the AT command +WIOCFG.
c. To enable use of UART_DTR to keep the module in active/idle state, issue the AT command +KSLEEP with the <mngt> parameter set to 0. When this is enabled, the module will stay in active/idle state while UART_DTR is low (active). For details, refer to *[1] RC71xx AT Command Reference (Doc# 41114675).*

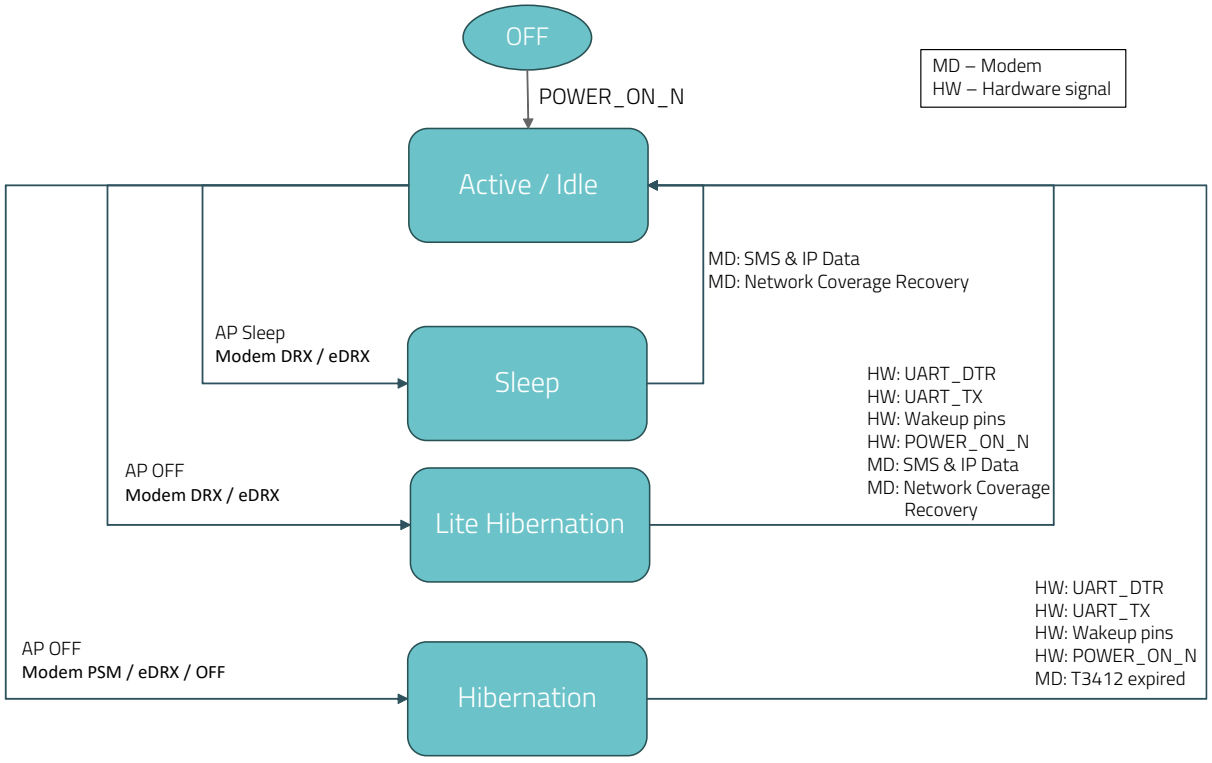


Figure 3-4: Power Mode State Machine

3.2.4 Power Saving Mode (PSM)

Power Saving Mode (PSM) is a 3GPP feature that allows the RC71xx to minimize power consumption by registering on a PSM-supporting LTE network, entering a very low power 'dormant' state for a pre-configured duration (via a periodic TAU (Tracking Area Update) timer), and then booting up for a short period to transmit/receive data, before re-entering PSM.

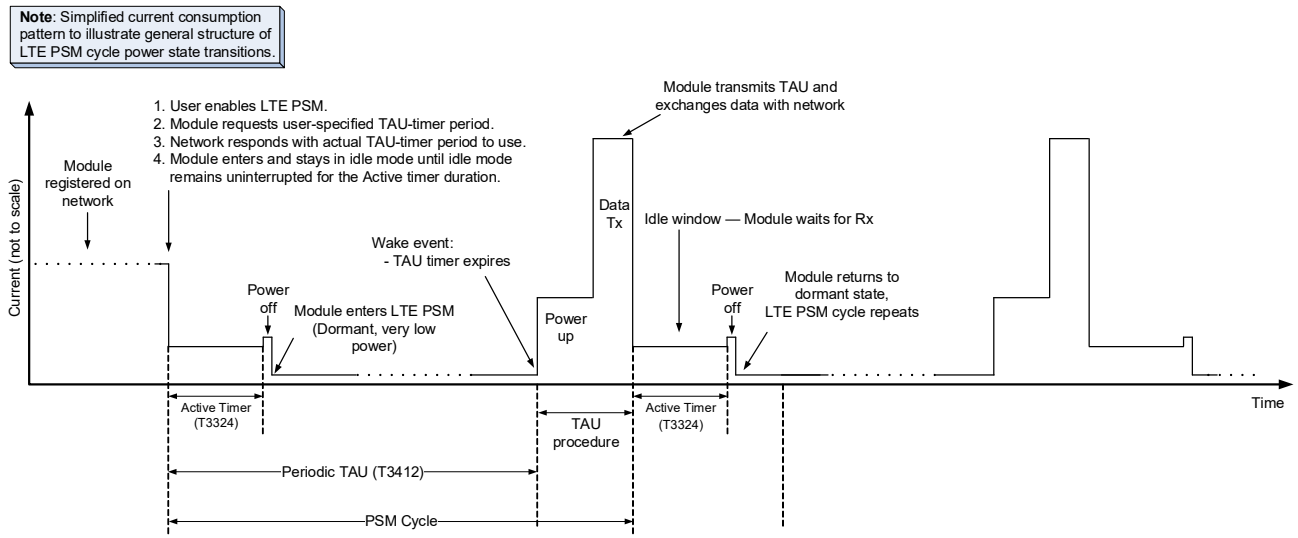


Figure 3-5: PSM Example (Simplified)

Typical candidates for PSM are systems (such as monitors and sensors) that:

- Require long battery life (low power consumption)
- Tolerate very long latency for mobile-terminated SMS/data
- Send and/or receive data infrequently and periodically (e.g., on a given schedule of once every few hours, days, weeks, etc.)

For example, a module connected to a sensor can be configured to:

- Wake periodically to transmit collected data to a server or network entity.
- Wait a short (configured) period of time to receive transmissions (e.g., 60 seconds) and then return to its dormant state.

Table 3-7 on page 21 describes the available triggers for waking an RC71xx from PSM. These triggers are configured using the methods described in Table 3-9.

Table 3-9: PSM-Related Application User Commands/Interfaces

Type	Command/Interface[a]	Description
AT	**+CPSMS**	3GPP-defined command (3GPP TS27.007 Release 12) that allows direct control of all LTE PSM parameters, and is useful for advanced users wanting to test/experiment with different options. This command is limited to networks that support PSM. It is not expected that every user must be fully versed in the details of PSM to take advantage of its capabilities. Use this command to: ▪ Enable/disable LTE PSM. ▪ Configure Periodic TAU timer (T3412) with a requested maximum duration of the dormant period. ▪ Configure Active timer (T3324) with a requested 'idle mode time' (the duration the module remains idle before going dormant). ▪ This command follows the 3GPP TS 27.007, Release 12 specification, with exceptions noted for certain parameters. *Note: The requested timer values are negotiated with the network and the final negotiated values take effect immediately, then persist across power cycles (e.g., after a power cycle, the settings will be used during network attach).*
	!POWERMODE	Custom Sierra Wireless command that allows application developers to enable PSM without the complexity of the **AT+CPSMS** syntax
	!POWERWAKE	Custom Sierra Wireless command used to configure PSM timers (TAU time, active time) in seconds. Note that only timer values supported by the 3GPP standard are allowed.
	*Note: **AT!POWERWAKE** (configuration of PSM timers) should be used with **AT!POWERMODE** (activation of the PSM feature). Using these proprietary SWI commands is equivalent to using the 3GPP **AT+CPSMS** command. **AT+CPSMS** will automatically change settings in **AT!POWERMODE**/**AT!POWERWAKE** and vice versa. As soon as the network accepts the PSM feature based on these command settings, the PSM power state will be activated in the RC71xx module (see Table 3-6 for details).*	

a. For AT command details, refer to *[1] RC71xx AT Command Reference (Doc# 41114675)*, available at source.sierrawireless.com.

PSM Process Example

The following example describes how the module uses PSM:

1. Module registers on an LTE network.
2. User enables PSM via AT command or API library function, specifying the desired TAU timer and Active timer periods, and optional wakeup sources.
3. Module submits the PSM request (including desired TAU timer) to the network.
4. Network responds and indicates whether PSM is supported and (if it is) indicates the actual TAU timer to use.

5. If the network supports PSM:
    a. Module enters idle mode (waiting for Rx from network).
    b. When module has remained idle for the Active timer period, module powers off (except for maintaining timer and interrupts) and enters PSM.

Note: If traffic must be transmitted when the module is in the sleep portion of the cycle, the module can initiate data/SMS session immediately.

    c. Module powers up before TAU timer expires, then transmits TAU and/or exchanges data with network.
    d. Module enters idle mode and cycle repeats.

Note: When the module is powered up, the PSM request can be re-issued with different timers and triggers to adjust the PSM behavior. These new settings take effect immediately.

Important Notes

- Carefully select the PSM Periodic-TAU timer and Active Time values to match the intended use case(s) for the module:
    - Periodic TAU PSM Cycle timer (T3412) — Note that while the module is dormant (for the duration of this timer), it will be completely unreachable by the network.
    - Active Time (Idle mode time after transmission (T3324)) — Make sure to set the Active timer high enough to provide appropriate delay-tolerance for mobile-terminated/network-originated transmissions to be received.
- When using multiple devices, consider scheduling the modules to wake at different times so that the network does not get flooded by all modules waking and transmitting simultaneously.

3.2.5 Active State to PSM Transition

If the module will be used in situations where it needs to be active very infrequently (for example, in a remote monitoring station that must transmit data periodically—e.g., on a regular schedule ranging from days to weeks or more), PSM may be used to reduce power consumption much more than is possible in Sleep state. If the module does not enter PSM, the request must be explicitly repeated—the module will not attempt to enter PSM automatically.

3.2.6 Extended Discontinuous Reception (eDRX)

The RC71xx supports eDRX, which is a 'flexible sleep' active mode that allows for longer sleep duration ($T_{I\text{-}eDRX}$) and a significant decrease in power consumption compared to regular DRX ($T_{I\text{-}DRX}$).

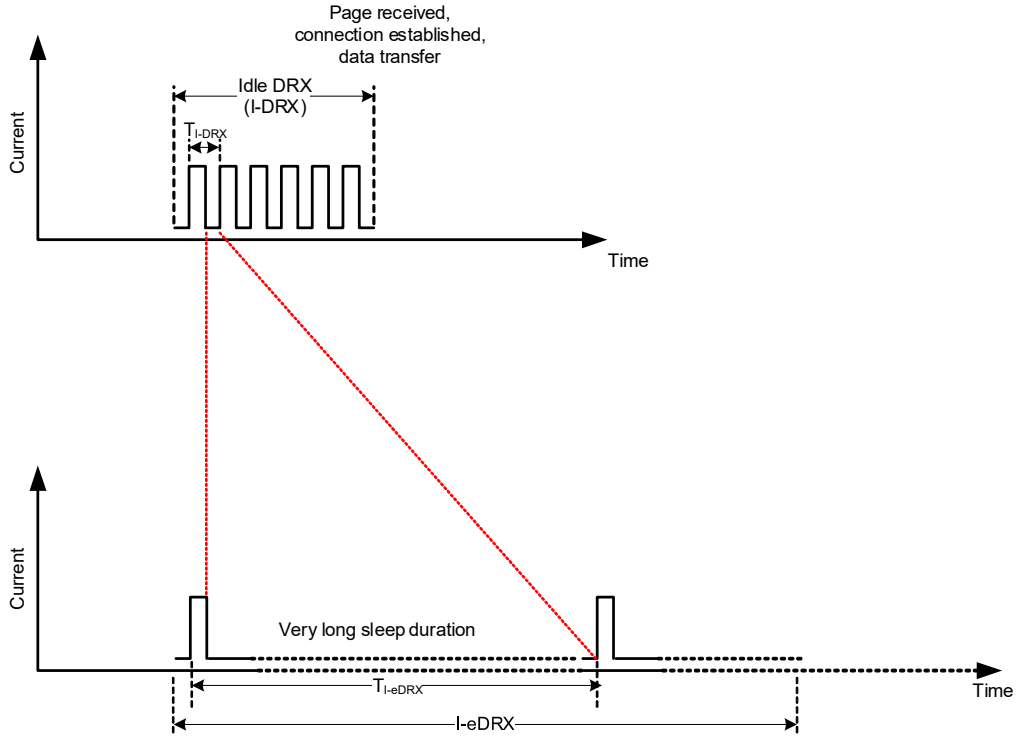


Figure 3-6: eDRX Example (Simplified)

Specifically, the RC71xx supports eDRX, which extends the DRX cycle (the paging cycle comprised of a paging window during which the module is awake and able to receive or transmit on the network, and a sleep period during which the network cannot wake the module) by increasing the sleep duration beyond the DRX maximum of 2.56 seconds:

- I-eDRX (Idle mode eDRX) — The sleep duration of the DRX cycle can be set up to 44 minutes.

Note: If traffic must be transmitted when the module is in the sleep portion of the cycle, the module can initiate data/SMS session immediately.

Table 3-10 describes the available methods for configuring eDRX.

Table 3-10: eDRX-Related Commands[a]

Type	Command	Description
AT	**+CEDRXS**	Enable/disable eDRX, and configure related settings
AT	**+CEDRXRDP**	Display current eDRX settings

a. For AT command details, refer to *[1] RC71xx AT Command Reference (Doc# 41114675)*, available at source.sierraw-ireless.com.

3.2.6.1 eDRX Process Example

- Use the **AT+CEDRXS** command to configure the desired eDRX behavior.
- During the network attachment process:
  - eDRX request and settings are sent to the network.
  - Network responds and indicates whether eDRX is supported for the connection and may adjust the eDRX parameters.
- If eDRX is supported by the network:
  - While in active mode (connected), the sleep duration is used if supported, otherwise the regular DRX sleep duration is used.
  - While in idle mode, the I-eDRX sleep duration is used if supported, otherwise the network uses the standard LTE I-DRX value.

3.2.6.2 Important Notes

- The sleep duration must be carefully selected to match the intended use case(s) for the module. While the module is asleep, it will be unreachable by the network. The duration should provide appropriate delay-tolerance for mobile-terminated/network-originated transmissions to be received.
- Network-side store and forward is supported — Packets will be stored until the module is reachable.

3.2.7 Current Consumption

The following tables describe the Sierra Wireless RC71xx module's current consumption under various power states. Typical values are measured at nominal supply voltage, nominal ambient temperature, and with a conducted 50 Ω load on the antenna port.

Note: All current consumption values are tested on the Sierra Development Kit.

Table 3-11: RC7110 Current Consumption Values

Power State	Details		Min[a,b]	Typ[a,c]	Max[d,c]	Units
Active						
LTE Data transfer[e]	B2		170	682	800	mA
	B4		170	630	750	mA
	B8		160	600	700	mA
	B12		160	590	680	mA
	B13		160	560	660	mA
	B66		170	650	750	mA
Idle — LTE	▪ Registered ▪ Paging cycle=256	USB active	—	28	—	mA
Airplane mode[f]	▪ Radio off	USB active	—	27	—	mA

Table 3-11: RC7110 Current Consumption Values (Continued)

Power State	Details		Min[a,b]	Typ[a,c]	Max[d,c]	Units
Sleep1						
Idle — LTE	▪ Registered ▪ Paging cycle=256	USB-SS	—	1.7	—	mA
Idle — LTE eDRX[g]	▪ Period: 40.96 sec	USB-SS	—	1.2	—	mA
Airplane mode[f]	▪ Radio off	USB-SS	—	0.6	—	mA
Sleep2 (Lite Hibernate)[h]						
Idle — LTE	▪ Registered ▪ Paging cycle=256	USB OFF[i]	—	350	—	µA
Idle — LTE eDRX[g]	▪ Period: 40.96 sec	USB OFF[i]	—	200	—	µA
Airplane mode[f]	▪ Radio off	USB OFF[i]	—	60	—	µA
Low Power Mode						
PSM Dormant (Hibernate)[h]	Non-active		—	9.5	—	µA
OFF (VBATT_ON)	Non-active		—	6	–	µA

a. Input 3.7 V, normal temperature
b. Tx power min = 0 dBm
c. Tx power max = 23 dBm
d. Input 3.4 V, 70°C
e. Bandwidth 10 MHz, UP/DL RB=50, enable throughput, modulation:QPSK
f. Radio is turned off and all interface settings are default without any external control connection.
g. eDRX test condition: eDRX setting: **`AT+CEDRXS=1,4,"0011"`**, eDRX period = 40.96 sec, PTW = 5.12 sec, DRX cycle = 64 ms. For AT command details, refer to *[1] RC71xx AT Command Reference (Doc# 41114675)*.
h. AT!CUSTOM="SIMPOWERSAVE",1 must be issued to enable the SIM to enter power saving mode when the module is in sleep state. If SIMPOWERSAVE=0, the module will not be able to enter Lite-Hibernate or Hibernate. For details, refer to *[1] RC71xx AT Command Reference (Doc# 41114675)*.
i. In Sleep2 (Lite Hibernate) mode, USB must be completely off. If VBUS power is connected on pin 16 (USB_VBUS), then VBUS power must also be turned off to prevent current leakage on the USB interface.

Table 3-12: RC7120 Current Consumption Values

Power State	Details		Min[a,b]	Typ[a,c]	Max[d,c]	Units
Active						
LTE Data transfer[e]	B1		160	720	820	mA
	B3		160	690	800	mA
	B7		170	740	830	mA
	B8		160	600	700	mA
	B20		160	660	750	mA
	B28		160	650	750	mA
Idle — LTE	▪ Registered ▪ Paging cycle=256	USB active	—	28	—	mA
Airplane mode[f]	▪ Radio off	USB active	—	27	—	mA

Table 3-12: RC7120 Current Consumption Values (Continued)

Power State	Details		Min[a,b]	Typ[a,c]	Max[d,c]	Units
Sleep1						
Idle — LTE	▪ Registered ▪ Paging cycle=256	USB-SS	—	1.7	—	mA
Idle — LTE eDRX[g]	▪ Period = 40.96 sec	USB-SS	—	1.2	—	mA
Airplane mode[f]	▪ Radio off	USB-SS	—	0.6	—	mA
Sleep2 (Lite Hibernate)[h]						
Idle — LTE	▪ Registered ▪ Paging cycle=256	USB OFF[i]	—	350	—	µA
Idle — LTE eDRX[g]	▪ Period = 40.96 sec	USB OFF[i]	—	200	—	µA
Airplane mode[f]	▪ Radio off	USB OFF[i]	—	60	—	µA
Low Power Mode						
PSM Dormant (Hibernate)[h]	Non-active		—	9.5	—	µA
OFF (VBATT_ON)	Non-active		—	6	—	µA

a. Input 3.7V, normal temperature
b. Tx power min = 0 dBm
c. Tx power max = 23 dBm
d. Input 3.4V, 70°C
e. Bandwidth 10 MHz, UP/DL RB=50, enable throughput, modulation:QPSK
f. Radio is turned off and all interface settings are default without any external control connection.
g. eDRX test condition: eDRX setting: **`AT+CEDRXS=1,4,"0011"`**, eDRX period = 40.96 sec, PTW = 5.12 sec, DRX cycle = 64 ms. For AT command details, refer to *[1] RC71xx AT Command Reference (Doc# 41114675)*.
h. AT!CUSTOM="SIMPOWERSAVE",1 must be issued to enable the SIM to enter power saving mode when the module is in sleep state. If SIMPOWERSAVE=0, the module will not be able to enter Lite-Hibernate or Hibernate. For details, refer to *[1] RC71xx AT Command Reference (Doc# 41114675)*.
i. In Sleep2 (Lite Hibernate) mode, USB must be completely off. If VBUS power is connected on pin 16 (USB_VBUS), then VBUS power must also be turned off to prevent current leakage on the USB interface.

3.3 RF

This section presents the module's WWAN RF interface, and defines the specifications for the LTE interface.

Note: RF sensitivity values presented in this section are for soldered-down modules. Sensitivity values decrease for modules installed in snap-in sockets, which might prevent the module from meeting 3GPP minimum specifications.

Sierra Wireless RC71xx is designed to be compliant with 3GPP Release 14 standards; refer to Network Technology Specifications.

3.3.1 Supported RF Bands

Table 3-13: Supported LTE[a] Bands

	B1	B2	B3	B4	B7	B8	B12	B13	B20	B28	B66
RC7110	—	Y	—	Y	—	Y	Y	Y	—	—	Y
RC7120	Y	—	Y	—	Y	Y	—	—	Y	Y	—

a. LTE (Cat 1bis)

3.3.2 LTE RF Interface

This section presents the LTE RF specification for Sierra Wireless RC71xx modules.

3.3.2.1 Tx Output Power

The module's LTE maximum transmitter output power is specified in Table 3-14.

Table 3-14: RC7110 Conducted Tx Max Output Power Tolerances—LTE[a]

RF Band	Operating Condition	Min	Typ	Max	Units	Notes
B2	Normal (25°C)	21	23	24	dBm	Power class 3
B4	Normal (25°C)	21	23	24	dBm	Power class 3
B8	Normal (25°C)	21	23	24	dBm	Power class 3
B12	Normal (25°C)	21	23	24	dBm	Power class 3
B13	Normal (25°C)	21	23	24	dBm	Power class 3
B66	Normal (25°C)	21	23	24	dBm	Power class 3

a. Stated typical power tolerance satisfies 3GPP TS 36.521-1 requirements for normal (25°C).

Table 3-15: RC7120 Conducted Tx Max Output Power Tolerances—LTE[a]

RF Band	Operating Condition	Min	Typ	Max	Units	Notes
B1	Normal (25°C)	21	23	24	dBm	Power class 3
B3	Normal (25°C)	21	23	24	dBm	Power class 3
B7	Normal (25°C)	21	23	24	dBm	Power class 3
B8	Normal (25°C)	21	23	24	dBm	Power class 3
B20	Normal (25°C)	21	23	24	dBm	Power class 3
B28	Normal (25°C)	21	23	24	dBm	Power class 3

a. Stated typical power tolerance satisfies 3GPP TS 36.521-1 requirements for normal (25°C).

3.3.2.2 Rx Sensitivity

The module's LTE receiver sensitivity is specified in the following tables.

Table 3-16: RC7110 Conducted Rx Sensitivity—LTE Bands[ab]

LTE Bands		+25°C (dBm) Primary (Typical)	Class A (dBm) Primary (Typical)
B2	Full RB BW: 10 MHz[c]	-98	-97
B4		-98	-96.5
B8		-98	-96.5
B12		-97	-96
B13		-97.5	-96.5
B66		-98	-97

a. RF sensitivity values are for soldered-down modules.
b. Per 3GPP specification.
c. Sensitivity values scale with bandwidth: x_MHz_Sensitivity = 10_MHz_Sensitivity - 10×log(10 MHz/x_MHz)
Note: Bandwidth support is dependent on firmware version

Table 3-17: RC7120 Conducted Rx Sensitivity—LTE Bands[ab]

LTE Bands		+25°C (dBm) Primary (Typical)	Class A (dBm) Primary (Typical)
B1	Full RB BW: 10 MHz[c]	-97.5	-96
B3		-97	-96
B7		-95	-94
B8		-98	-96.5
B20		-97	-96.5
B28		-96	-95

a. RF sensitivity values are for soldered-down modules.
b. Per 3GPP specification.
c. Sensitivity values scale with bandwidth: x_MHz_Sensitivity = 10_MHz_Sensitivity - 10×log(10 MHz/x_MHz)
Note: Bandwidth support is dependent on firmware version

3.3.3 WWAN Antenna Interface

The following table defines the WWAN antenna interface of the Sierra Wireless RC71xx modules.

Table 3-18: WWAN Antenna Interface Pins

Pin #	Signal name	Direction	Function
48	GND		Primary Antenna Ground
49	RF_MAIN	Input/Output	Primary Antenna Interface

Table 3-18: WWAN Antenna Interface Pins (Continued)

Pin #	Signal name	Direction	Function
50	GND		Primary Antenna Ground
136	GND		Primary Antenna Ground
139	GND		Primary Antenna Ground

Note: For the routing of ground and RF signal, see Figure 5-4 and Figure 5-5.

3.3.3.1 WWAN Antenna Recommendations

Table 3-19 defines the key characteristics to consider for antenna selection.

Table 3-19: Antenna Recommendations[a]

Parameter		Recommendations	Notes
Antenna system		External multi-band antenna system	Single WWAN antenna (Antenna 1)[b]
Operating bands	RC7110	617–894 MHz	Operating bands depend on the module's supported bands/modes.
		1710–2200 MHz	
	RC7120	703–960 MHz	
		1710–2170 MHz	
		2500–2690 MHz	
VSWR		< 2.5:1 (worst case)	▪ On all bands including band edges ▪ Applies to MAIN antenna
Total radiated efficiency		> 50% on all bands	▪ Measured at the RF connector. ▪ Applies to MAIN antenna ▪ Includes mismatch losses, losses in the matching circuit, and antenna losses, excluding cable loss. ▪ Sierra Wireless recommends using antenna efficiency as the primary parameter for evaluating the antenna system. ▪ Peak gain is not a good indication of antenna performance when integrated with a host device (the antenna does not provide omnidirectional gain patterns). Peak gain can be affected by antenna size, location, design type, etc. — the antenna gain pattern remains fixed unless one or more of these parameters change.
Radiation patterns		Nominally omnidirectional radiation pattern in azimuth plane.	
Mean Effective Gain (MEG)		≥ -3 dBi	

Table 3-19: Antenna Recommendations[a] (Continued)

Parameter	Recommendations	Notes
Maximum antenna gain	Must not exceed antenna gain due to RF exposure and ERP/EIRP limits, as listed in the module's FCC grant.	
Maximum voltage applied to antenna	6.3 VDC	

a. The worst-case VSWR figure for the transmitter bands may not guarantee RSE levels to be within regulatory limits. The device alone meets all regulatory emissions limits when tested into a cabled (conducted) 50 Ω system. With antenna designs with up to 2.5:1 VSWR or worse, the radiated emissions could exceed limits. The antenna system may need to be tuned in order to meet the RSE limits as the complex match between the module and antenna can cause unwanted levels of emissions. Tuning may include antenna pattern changes, phase/delay adjustment, passive component matching.
b. Antenna 1 — Primary (RF_MAIN)

3.4 Electrical Specifications

This section provides details of key electrical specifications.

3.4.1 Absolute Maximum Ratings

Warning: *If these parameters are exceeded, even momentarily, damage may occur to the device. In addition, extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.*

Note: Operation above the maximum specified operating voltage (see Table 3-3) is not recommended, and specified typical performance or functional operation of the device is neither implied nor guaranteed.

Table 3-20: Absolute Maximum Ratings

Parameter		Min	Typ	Max	Units
Power supply voltages					
VBAT_BB	Power Supply Input	0	–	5.0	V
VBAT_RF	Power Supply Input	0	–	5.0	V
VDD_Px (low-voltage (1.8 V) operation)	Digital pad circuits	-0.5	–	2.3	V
VDD_Px (high-voltage (3 V) operation)	Digital pad circuits	-0.5	–	3.35	V
USB signal pins					
USB_D+	High-speed USB data plus	–	–	3.6	V
USB_D-	High-speed USB data minus	–	–	3.6	V
USB_VBUS	High-speed USB bus voltage	–	–	5.25	V
Thermal conditions					
TS	Storage temperature	-40		85	°C
TJ	Junction temperature	–	–	92	°C

Table 3-20: Absolute Maximum Ratings (Continued)

Parameter		Min	Typ	Max	Units
Maximum voltage applied to antenna interface pins					
VANT	RF_MAIN	–		6.3	Vdc
ESD ratings					
See EMC and ESD Recommendations.					

3.4.2 Digital I/O Characteristics

Table 3-21 links to specific tables describing I/O characteristics for supported digital interfaces.:

Table 3-21: Digital Interface Characteristics — Summary

Interface(s)		Table 3-22: Digital I/O Characteristics — VDD_IO = 1.80 V (nominal)	Table 3-23: Digital I/O Characteristics — VDD_IO = 3.30 V (nominal)	Table 3-24: Digital Output Characteristics — VDD_IO = 1.80 V (nominal)	Table 3-25: Digital Input Characteristics — VDD_IO = 1.80 V (nominal)	Table 3-26: Digital I/O Characteristics — Dual-voltage VUIM_IO = 1.80 V or 3 V (nominal)
GPIOs	GPIO2, GPIO21	Y[a]	Y[a]	—	Y[a]	—
	GPIO4, GPIO42	—	—	—	Y	—
	All other GPIOs	Y	Y	—	—	—
UART1	UART1_DTR	—	—	—	Y	—
	All other UART1_*	Y	Y	—	—	—
UART2	All UART2_*	Y	Y	—	—	—
UIM1	UIM1_DET	—	—	—	Y	—
	All other UIM1_*	—	—	—	—	Y
UIM2	UIM2_DET	—	—	—	Y	—
	All other UIM2_*	Y	—	—	—	—
ANT_CNTL	All ANT_CNTL*	—	—	Y	—	—
Control signals	RESET_OUT_N, SAFE_PWR_REMOVE, TP1, WAKE_ON_WWAN, W_DISABLE_N, WWAN_LED_N	Y	Y	—	—	—

a. GPIO2 and GPIO21 use Table 3-22 and Table 3-23 when configured for GPIO mode, or Table 3-25 when configured as wakeup sources.

Table 3-22: Digital I/O Characteristics — V_{DD_IO} = 1.80 V (nominal)[a] [b]

Parameter		Notes	Min	Max	Units
V_{IH}	High level input voltage	CMOS/Schmitt	0.7 × V_{DD_IO}	V_{DD_IO} + 0.3	V
V_{IL}	Low level input voltage	CMOS/Schmitt	-0.3	0.2 × V_{DD_IO}	V
V_{SHYS}	Schmitt hysteresis voltage		62	111	mV
V_{OH}	High level output voltage	CMOS, at pin-rated drive strength	V_{DD_IO}- 0.45	V_{DD_IO}	V
V_{OL}	Low level output voltage	CMOS, at pin-rated drive strength	0	0.45	V
R_U	Pull-up resistance		117	331	kΩ
R_D	Pull-down resistance		91	291	kΩ
I_{IH}	Input high leakage current[c]	No pull-down	-10	10	?A
I_{IL}	Input low leakage current[d]	No pull-up	-10	10	?A
C_{IN}	Input capacitance[e]		–	3.5	pF
I_{PIN}	Current per pin		–	10	mA

a. This table applies to the following interfaces when pin 145 (IO_VOL_SEL) is floating:
- GPIOs (all signals except GPIO4, GPIO42). Note: Applies to GPIO2 and GPIO21 only when configured for GPIO mode using AT+WIOCFG — if GPIO2/GPIO21 are configured as wakeup input pins (default), Table 3-25 applies.
- UART1 (all signals except UART1_DTR)
- UART2 (all signals)
- UIM2 (all signals except UIM2_DET)
- Control signals/indications: RESET_OUT_N, SAFE_PWR_REMOVE, TP1, WAKE_ON_WWAN, W_DISABLE_N, WWAN_LED_N

When pin 145 (IO_VOL_SEL) is connected to ground, Table 3-23 applies to the interfaces above.

b. When pin 145 (IO_VOL_SEL) is floating, all signals in footnote (a) support 1.8 V.

c. Pin voltage = V_{DD_IO}. For keeper pins, pin voltage = V_{DD_IO} - 0.45.

d. Pin voltage = GND and supply = V_{DD_IO}. For keeper pins, pin voltage = 0.45 V and supply = V_{DD_IO}

e. Input capacitance is guaranteed by design.

Table 3-23: Digital I/O Characteristics — V_{DD_IO} = 3.30 V (nominal)[a]

Parameter		Notes	Min	Max	Units
V_{IH}	High level input voltage	CMOS/Schmitt	0.7 × V_{DD_IO}	V_{DD_IO} + 0.3	V
V_{IL}	Low level input voltage	CMOS/Schmitt	-0.3	0.2 × V_{DD_IO}	V
V_{SHYS}	Schmitt hysteresis voltage		121	181	mV
V_{OH}	High level output voltage	CMOS, at pin-rated drive strength	0.8 × V_{DD_IO}	—	V
V_{OL}	Low level output voltage	CMOS, at pin-rated drive strength	0	0.15 × V_{DD_IO}	V
R_U	Pull-up resistance		58	133	kΩ
R_D	Pull-down resistance		52	128	kΩ
I_{IH}	Input high leakage current	No pull-down	-10	10	?A
I_{IL}	Input low leakage current	No pull-up	-10	10	?A
C_{IN}	Input capacitance[b]		–	3.5	pF
I_{PIN}	Current per pin		–	10	mA

a. This table applies to the following interfaces when pin 145 (IO_VOL_SEL) is connected to ground:
   - GPIOs (all signals except GPIO4, GPIO42).
     Note: Applies to GPIO2 and GPIO21 only when configured for GPIO mode using AT+WIOCFG. If GPIO2/GPIO21 are configured as wakeup input pins (default), Table 3-25 applies.
   - UART1 (all signals except UART1_DTR)
   - UART2 (all signals)
   - Control signals/indications: RESET_OUT_N, SAFE_PWR_REMOVE, TP1, WAKE_ON_WWAN, W_DISABLE_N, WWAN_LED_N

   When pin 145 (IO_VOL_SEL) is floating, Table 3-22 applies to the interfaces above.
b. Input capacitance is guaranteed by design.

Table 3-24: Digital Output Characteristics — V_{DD_IO} = 1.80 V (nominal)[a]

Parameter		Notes	Min	Max	Units
V_{OH}	High-level output voltage		0.8 × V_{DD_IO}	–	V
V_{OL}	Low-level output voltage		–	0.15 × V_{DD_IO}	V
$C_{I/O}$	I/O capacitance[b]		–	3.5	pF

a. Applies to ANT_CNTL0, ANT_CNTL1
b. Input capacitance is guaranteed by design.

Table 3-25: Digital Input Characteristics — V_{DD_IO} = 1.80 V (nominal)[a]

Parameter		Notes	Min	Max	Units
V_{IH}	High level input voltage	CMOS/Schmitt	1.4	2.1	V
V_{IL}	Low level input voltage	CMOS/Schmitt	-0.3	0.42	V
V_{SHYS}	Schmitt hysteresis voltage		200	–	mV
R_P	Pull-up resistance		170	230	kΩ
I_{IH}	Input high leakage current[b]	No pull-down	–	0.3	?A
I_{IL}	Input low leakage current[c]	No pull-up	-10	–	?A
I_{PIN}	Current per pin		-	10	mA
C_{IN}	Input capacitance[d]		1.5	2	pF

a. Applies to:
   - GPIO42
   - GPIO2 and GPIO21 in their default configuration as wakeup input pins.
     Note: If GPIO2/GPIO21 are configured as for GPIO mode using AT+WIOCFG, Table 3-22, Table 3-23 and Table 3-25 apply.
   - UIM1_DET, UIM2_DET/GPIO4, UART1_DTR
b. Pin voltage = V_{DD_IO}
c. Pin voltage = GND and supply = V_{DD_IO}
d. Input capacitance is guaranteed by design.

Table 3-26: Digital I/O Characteristics — Dual-voltage V_{UIM_IO} = 1.80 V or 3 V (nominal)[a]

Parameter		Notes	Min	Max	Units
Common to UIM dual-voltage pads (1.8 V/3 V)					
V_{IH}	High level input voltage	CMOS/Schmitt	0.7 × V_{UIM_IO}	V_{UIM_IO} + 0.3	V
V_{IL}	Low level input voltage	CMOS/Schmitt	-0.3	0.2 × V_{UIM_IO}	V
V_{SHYS}	Schmitt hysteresis voltage		62	111	mV

Table 3-26: Digital I/O Characteristics — Dual-voltage V_{UIM_IO} = 1.80 V or 3 V (nominal)[a] (Continued)

Parameter		Notes	Min	Max	Units
V_{OH}	High level output voltage	CMOS, at pin-rated drive strength	0.8 × V_{UIM_IO}	–	V
V_{OL}	Low level output voltage	CMOS, at pin-rated drive strength	0	0.45	V
R_P	Pull-up resistance	Pull-up	117	331	kΩ
R_D	Pull-down resistance	Pull-down	91	291	kΩ
$C_{I/O}$	I/O capacitance[b]		–	3.5	pF
I_{IH}	Input high leakage current[c]	No pull-down	–	10	?A
I_{IL}	Input low leakage current[d]	No pull-up	-10	–	?A

a. Applies to UIM1 (all signals except UIM1_DET)
b. Input capacitance is guaranteed by design.
c. Pin voltage = V_{UIM_IO}
d. Pin voltage = GND and supply = V_{UIM_IO}

3.4.3 Internal Devices

Table 3-27 summarizes the frequencies generated within the Sierra Wireless RC71xx. This table is provided for reference only to the device integrator.

Table 3-27: Internal Device Frequencies

Subsystem / Feature	Frequency	Units
Real Time Clock	32.768	kHz
Fundamental clock	26	MHz
USB	480	Mb/s

3.5 Processing

3.5.1 Application Processor

The Application Processor (AP) is based on a Cortex-M3 32-bit RISC architecture core. It has the following main characteristics:

- Up to 204 MHz operation
  - Supported frequencies: 204 MHz, 102 MHz, 26 MHz

Refer to Interfaces Specifications for the list of interfaces supported by this core.

3.5.2 Embedded Memory

The Sierra Wireless RC71xx module includes NOR Flash and SRAM embedded memory as detailed in Table 3-28.

Refer to the latest customer release note for any changes regarding embedded memory.

Table 3-28: Embedded Memory Details

Type	Details	Size
NOR Flash	Application Processor (AP) Flash	4 MB
	Communication Processor (CP) Flash	1 MB
SRAM	ASMB is used for AP	64 KB
	MSMB is shared for AP and CP	1.25 MB

Flash memory is partitioned for use by various elements:

- AP Flash — Can be used by the FreeRTOS firmware, framework, and application.
- CP Flash — Provided for modem use.

3.5.3 Secure Boot

Sierra Wireless RC71xx modules incorporate the following permanently enabled feature to enhance device security:

- Secure Boot—Ensures only firmware images signed by Sierra Wireless can be loaded and run on the RC71xx modules. Specifically, Secure Boot applies to the following firmware components: system boot loader, AP image firmware, and CP modem image firmware.

3.6 Mechanical Drawing

The Sierra Wireless RC71xx module's LGA footprint is a 239-pad array of copper pads (see Physical Dimensions and Connection Interface). The following drawing illustrates the device footprint and dimensions.

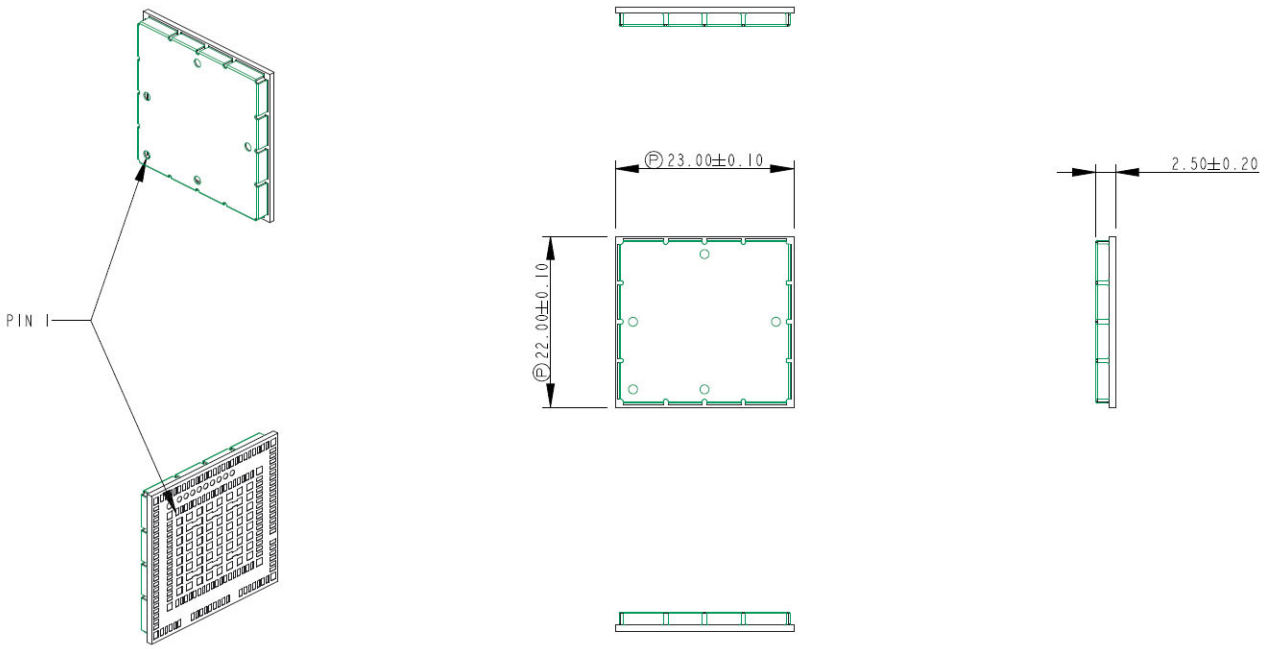


Figure 3-7: Mechanical Drawing 1

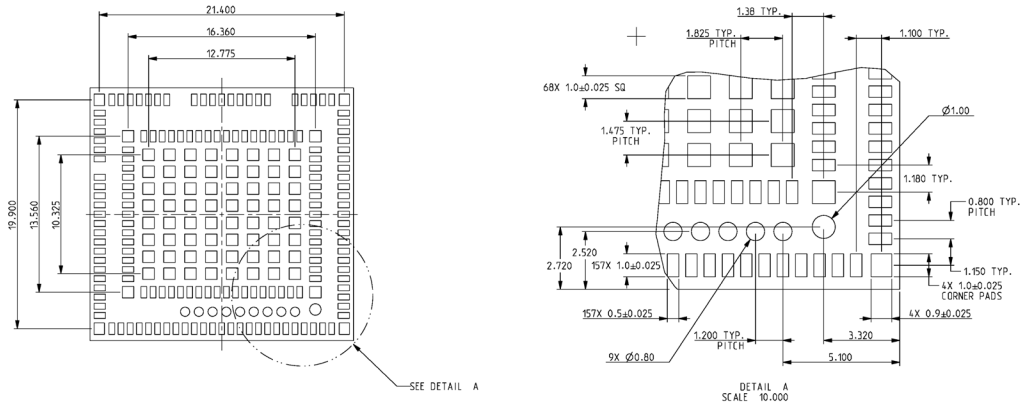


Figure 3-8: Mechanical Drawing 2

3.7 Mechanical Specifications

The following table describes additional mechanical specifications for the Sierra Wireless RC71xx module.

Table 3-29: Mechanical Specifications

Specification	Value	Notes
Clamping force	20 psi	Maximum clamping force on module over entire shield surface.

4: Interfaces Specifications

This section describes the interfaces supported by the Sierra Wireless RC71xx embedded module and provides specific voltage, timing, and circuit recommendations for each interface.

4.1 POWER_ON_N

The Sierra Wireless RC71xx module requires a low level signal (POWER_ON_N) that is used to switch the module ON or OFF.

To turn the module ON:

- Power the module (VBATT on) and connect POWER_ON_N to ground for at least 200 ms.

To turn the module OFF:

- While the module is in an active power state mode, assert POWER_ON_N to low for more than 2 seconds.
  (Note — The module can also be turned off using an AT command. See Software-Initiated Power Down.)

Important: *Any sudden power cut to the embedded module while the module is powered (i.e., removing VBATT while powering on, operating normally, and powering down) increases the risk of a non-volatile memory (NVM) crash.*

To prevent any unexpected exceptions or NVM crashes, the customer must execute the power down sequence described in Software-Initiated Power Down.

If the firmware has become corrupted (due to improper shutdown or other causes) and boots abnormally, a full firmware update is required to replace the corrupt firmware, using one of the following methods:

- *Use the TP1 pin to install a full firmware update via the USB Serial COM port — see TP1 (Boot Pin).*
- *Use the UART1 interface to install a full firmware Update.*
  For details, refer to [3] RC71xx Linux Host Tools User Guide (Doc# 41114711) or
  [4] RC71xx Windows Host Tools User Guide (Doc# 41114805) depending on the host platform.

Table 4-1 describes the POWER_ON_N signal's characteristics.

Table 4-1: POWER_ON_N Electrical Characteristics[a]

Parameter	Min	Typ	Max	Units
Input Voltage — Low		–	0.35	V
Internal pull-up resistor		150		kΩ

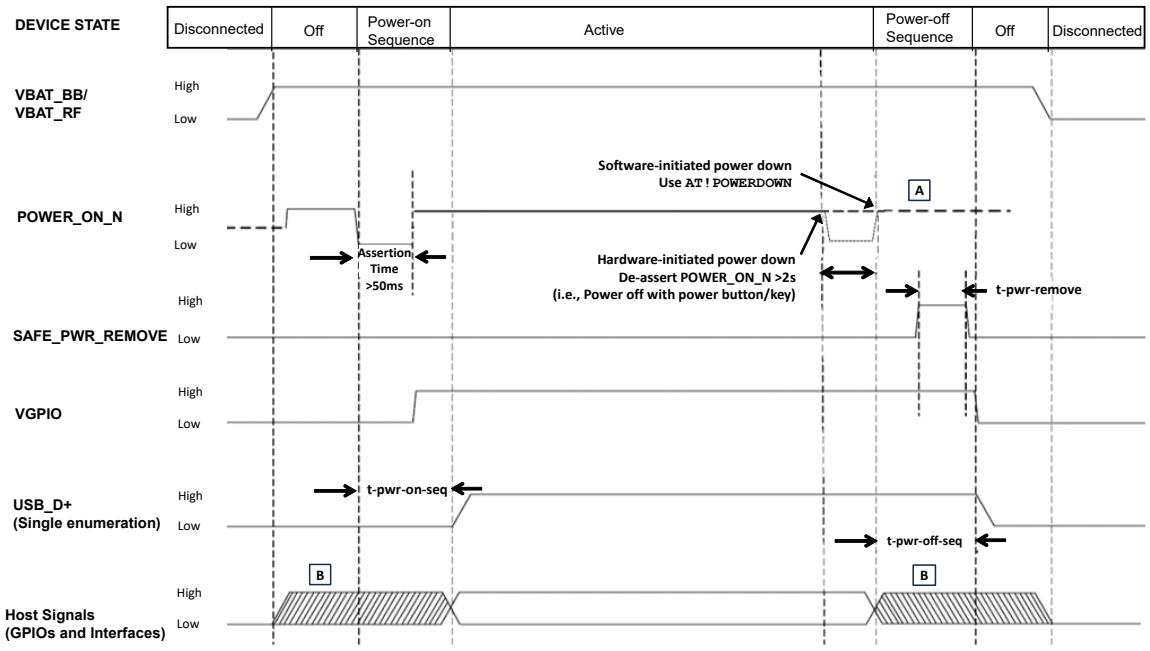
a. When floating, voltage will be approximately 2 V.

4.1.1 Power-up Sequence

4.1.1.1 Power On / Off Timing

The host device should not drive any signals to the module until VGPIO rises (approximately 250 ms after power-up). Before reaching the Active power state, signals on the host port must be set to floating, High-Z, or input pull-down. This setting also applies when the module is in reset mode, during a firmware update, or during a power-off sequence. The host must consider this signal setting when designing the module interface.

Figure 4-1 describes the timing sequence for powering the module on and off.



A After initiating the power down using AT!POWERDOWN, the host should ensure that all I/Os that are connected to the module are set to High-Z, floating or input pull-down, before the VGPIO switches off.

B When the module is not in the Active state (i.e., is powered on), the host should ensure that all I/Os that are connected to the module are set to High-Z, floating, or input pull-down.

Figure 4-1: Signal Timing (POWER_ON_N, and USB Enumeration)

Table 4-2: POWER_ON_N Timing Parameters

Parameter	Typical	Maximum	Units
t_pwr_on_seq	1.6	2	s
t_pwr_off_seq	0.5	2	s
t_pwr_remove	13	—	ms
POWER_ON_N assertion time[a]	0.200	1	s

a. Assertion time is the time required to keep POWER_ON_N at LOW level to ensure themodule can be powered ON successfully.

4.1.1.2 USB Enumeration

The module supports single USB enumeration with the host. Enumeration starts within t_pwr_on_seq (maximum) seconds of power-on.

4.1.2 Software-Initiated Power Down

To power down the module via software:

1. Initiate the power down process:
   ```
   AT!POWERDOWN
   ```
2. Monitor VGPIO and SAFE_PWR_REMOVE.
3. When both VGPIO and SAFE_PWR_REMOVE are on the low level, remove power.

Note: If the VGPIO cannot be monitored from the design interface, measure the delay time (pulse from SAFE_PWR_REMOVE to VGPIO must = 0, refer to Figure 4-8 for details) and include this information in the firmware to ensure that power can be removed safely.

4.2 POWER_ON_N, RESET_IN_N, AT!POWERDOWN Use Cases

Table 4-3 lists the behavior of the RC71xx depending on POWER_ON_N, RESET_IN_N and **AT!POWERDOWN** use cases.

Table 4-3: POWER_ON_N, RESET_IN_N and AT!POWERDOWN Use Cases

Use Case		Behavior
POWER_ON_N	VBATT is applied then POWER_ON_N is asserted	Turns ON
	POWER_ON_N is asserted then VBATT is applied	Turns ON
	After module turns on, POWER_ON_N is asserted > 2 seconds	Turns OFF
RESET_IN_N[a]	In Power ON state, RESET_IN_N is asserted	Hardware resets
AT!POWERDOWN	POWER_ON_N is de-asserted then the power OFF command is sent	Turns OFF

a. This pin should only be used for emergencies such as when the module stops responding to AT commands.

4.3 USB

The Sierra Wireless RC71xx implements a high-speed USB 2.0 Interface, which conforms to *Universal Serial Bus Specification, Revision 2.0.*

Note: It is strongly recommended to make the USB interface accessible through test points..

Table 4-4: USB Pin Descriptions

Pin	Signal Name	Direction	Function
12	USB_D-	Input/Output	Differential data interface negative
13	USB_D+	Input/Output	Differential data interface positive
16	USB_VBUS	Input	USB supply voltage

Table 4-5: USB_VBUS Characteristic

USB		Value	Units
USB_VBUS	Voltage range	4.75–5.25 or VBAT_BB	V
	Maximum Current Drawn	1	mA
	Maximum Input Capacitance (Min ESR = 50 mΩ)	10	µF

Note: The USB interface has routing constraints. For details, refer to USB Interface.

Note: If USB_VBUS is high (i.e., connected to VBAT, or connected to VBUS from USB) when the module is being powered down, the module will automatically reboot. To prevent automatic rebooting, make sure USB_VBUS is disconnected when powering down.

4.4 UART

The Sierra Wireless RC71xx provides two UART interfaces:

- UART1 (primary UART) — 8-wire interface. This interface is used for data communication between the module and a PC or host processor.
- UART2 (secondary UART) — 4-wire interface. This interface is used for transmitting module logs to a PC or host processor.

Both interfaces (UART1, UART2) comply with the RS-232 interface.

Supported baud rates (bps):

- UART1 — 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600
- UART2 — 921600

Flow control is managed using the UART_RTS and UART_CTS signals.

Table 4-6 describes the signals used for UART1 and UART2.

Note: UART signals are named with respect to the host device, and directions are listed with respect to the module. For example, UART1_RX is an output from the module to the host.
WIFI coex and 8-wire UART concurrency is not supported.

Table 4-6: UART Pins

Pin	Interface	Name[a]	Direction[b]	Function	Reset State	If Unused	Notes
2	UART1	UART1_RI[c]	Output	Ring Indicator Signal incoming calls, SMS, etc.	Pull Down	Leave open	Do not install external pull-up on this pin, otherwise the module will not boot.
3		UART1_RTS[d]	Input	Ready To Send, Flow Control	Pull Down		Highly Recommended
4		UART1_CTS[d]	Output	Clear To Send, Flow Control	Pull Down		Highly Recommended
5		UART1_TX[d]	Input	Transmit Data	Pull Down		Highly Recommended
6		UART1_RX[d]	Output	Receive Data	Pull Down		Highly Recommended
7		UART1_DTR[e]	Input (active low)	Data terminal ready Prevents the RC71xx from entering sleep mode, switches between data mode and command mode, and wakes the module.	Pull Down	Leave open	
8		UART1_DCD	Output	Data Carrier Detect Signal data connection in progress	Pull Down	Leave open	Do not install external pull-up on this pin, otherwise the module will not boot.
9		UART1_DSR	Output	Data Set Ready Signal UART interface is ON	Pull Down	Leave open	Do not install external pull-up on this pin, otherwise the module will not boot.
96	UART2[d]	UART2_TX	Input	Transmit data	Pull Down		Highly Recommended
97		UART2_RX	Output	Receive data	Pull Down		Highly Recommended
98		UART2_RTS	Input	Ready To Send, flow control	Pull Down		Highly Recommended
99		UART2_CTS	Output	Clear To Send, flow control	Pull Down		Highly Recommended

a. Signals are named with respect to the host device. For example, UART1_RX is the signal used by the host to receive data from the module.
b. Signal direction with respect to the module. For example, UART1_RX is an output from the module to the host.
c. RI can be used independently and supports the following AT commands: **AT+WWAKESET** and **AT+WRID**.
d. Must be accessible through 0 Ω resistors. Test points are strongly recommended at module side.
e. Pin is 'wakeable'. Can be used to trigger the module to wake up from sleep state. For details, see Table 3-8: Modem Wakeup Sources (Hardware).

4.5 UIM Interface

The Sierra Wireless RC71xx has two physical UIM interfaces:
- UIM1 — This interface allows control of 1.8 V or 3 V UIMs.
- UIM2 — This interface allows control of 1.8 V UIMs only.

Note: UIM1 and UIM2 cannot be activated simultaneously (DSSS).

4.5.1 External UIM1 and UIM2 Interfaces

Table 4-7 describes the signals used for UIM1.

Table 4-7: UIM1 Interface Pins

Pin	Name	Direction[a]	Function	If Unused
26	UIM1_VCC	Output	Supply output (1.8V / 3V)	Leave open
27	UIM1_CLK	Output	Clock	Leave open
28	UIM1_DATA[b]	Input / Output	Data connection	Leave open
29	UIM1_RESET_N	Output	Reset	Leave open
64	UIM1_DET[c]	Input	Detect UIM	Leave open

a. Signal direction with respect to the module. Examples: UIM1_DET (pin 64) is an input to the module from the host; UIM1_RESET_N (pin 29) is an output from the module to the host.
b. UIM1_DATA has a 10 kΩ internal pull-up resistor (i.e., inside the module).
c. Pin is 'wakeable'. Can be used to trigger the module to wake up from sleep mode. For details, see Table 3-8: Modem Wakeup Sources (Hardware).

Table 4-8 describes the signals used for UIM2.

Table 4-8: External UIM2 Interface[a]

Pin	Name	Direction[b]	Function	If Unused
55	UIM2_VCC	Output	Supply output (1.8V)	Leave open
56	UIM2_DATA[c]	Input / Output	Data connection	
57	UIM2_RESET_N	Output	Reset	
58	UIM2_CLK	Output	Clock	
65	UIM2_DET[d]/GPIO4	Input	Detect UIM2	

a. UIM2 supports only 1.8V.
Note — If pin 145 (IO_VOL_SEL) is connected to ground (which selects 3.3 V), UIM2 will not be supported.
b. Signal direction with respect to the module. Examples: UIM2_DET (pin 65) is an input to the module from the host; UIM2_RESET_N (pin 57) is an output from the module to the host.
c. UIM2_DATA and UIM2_RESET_N have 10 kΩ internal pull-up resistors (i.e., inside the module).
d. Pin is 'wakeable'. Can be used to trigger the module to wake up from sleep mode. For details, see Table 3-8: Modem Wakeup Sources (Hardware).

4.5.2 External SIM Selection

Selecting an active SIM between UIM1 (external UIM1) and UIM2 (external UIM2) is possible using AT commands. Refer to *[1] RC71xx AT Command Reference (Doc# 41114675)* for more details regarding these commands

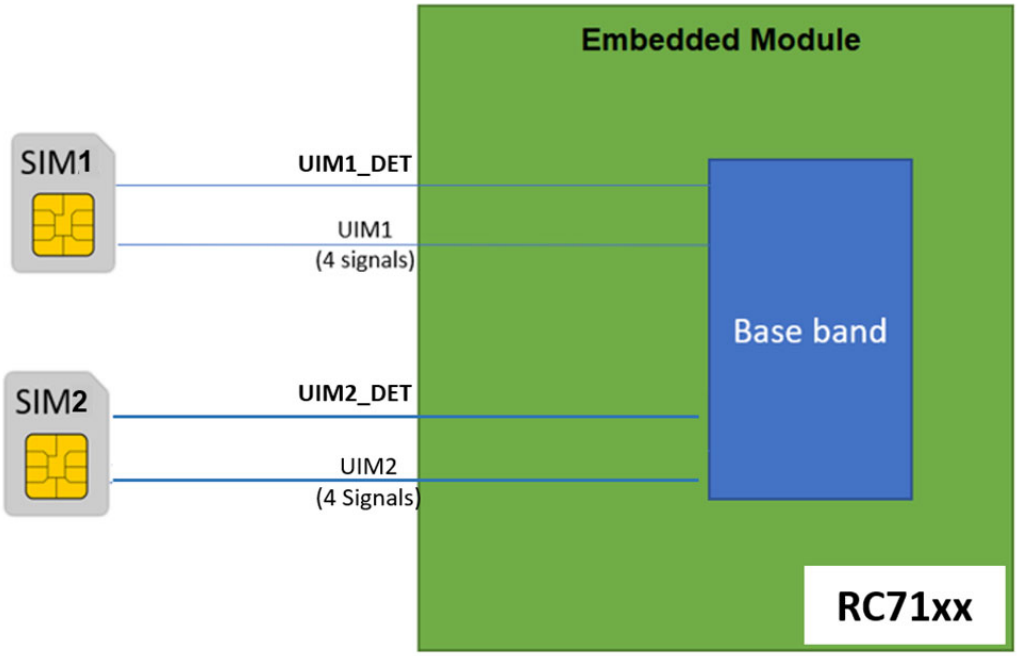


Figure 4-2: Dual External SIM Configuration

Note: Figure 4-2 illustrates the recommended implementation of the dual external SIM configuration. For a detailed UIM schematic, see Figure 5-8.

4.6 General Purpose Input/Output

The Sierra Wireless RC71xx defines several GPIOs for customer use, as described in Table 4-9. For electrical specifications, see Table 3-22.

Note: There should not be any voltage applied to the GPIOs when the module is off or resetting..

Table 4-9: GPIO Pin Description

Pin	Signal Name	Edge Wakeable	Default State	Function	If Unused
10	GPIO2[a]	Yes	PD	General purpose I/O	Leave open
40	GPIO7	—	PD	General purpose I/O	
41	GPIO8	—	PD	General purpose I/O	
46	GPIO6[b]	—	PD	General purpose I/O	
65	GPIO4[c]	Yes	PU	Input only	
109	GPIO42[a]	Yes	PU	Input only	
147	GPIO21[a]	Yes	PD	General purpose I/O	
148	GPIO22	—	PD	General purpose I/O	
149	GPIO23	—	PD	General purpose I/O	
150	GPIO24	—	PD	General purpose I/O	
155	GPIO30	—	PD	General purpose I/O	
156	GPIO31	—	PD	General purpose I/O	
159	GPIO25	—	PD	General purpose I/O	

a. Pin is 'wakeable'. Can be used to trigger the module to wake up from sleep mode. For details, see Table 3-8: Modem Wakeup Sources (Hardware).
b. See GPIO6.
c. See GPIO4.

4.7 GPIO4

GPIO4 can be used for two different functions as described below.

4.7.1 SIM Detect

GPIO4 can provide a detect function to the external UIM2 to detect the physical presence of a UIM card in the UIM holder. (Note — The module has an internal pull-up resistor on this signal; no external pull-up is needed.)

The UIM detect signal transitions:
- When a UIM is inserted — high (logic 0 to logic 1)
- When a UIM is removed — low (logic 1 to logic 0)

4.7.2 General Purpose Input Trigger Wakeup Source

To configure GPIO4 as a GPIO input trigger wakeup source:

1. Unlock the extended AT command set:
```
AT!ENTERCND="<key>"  ← <key> — Unlock key code
```

2. Disable the external SIM detect feature:
```
AT+CUSTOM="UIM2ENABLE",0
```
3. Configure GPIO4 as either:
   - a trigger falling wakeup source:
```
AT+WIOCFG=4,4[,0,,3,4]
```
   - a trigger rising wakeup source:
```
AT+WIOCFG=4,4,0,,1,3
```
4. Reboot the module:
```
AT!RESET
```

4.8 GPIO6

GPIO6 can be used as a general purpose input/output, or as a control signal to hold peripheral devices in reset, as described below. Refer to *[1] RC71xx AT Command Reference (Doc# 41114675)* for details.

4.8.1 GPIO6 — General Purpose Input / Output

To configure GPIO6 as a GPIO:

1. Configure GPIO6:
```
AT+WIOCFG=6,4
```
2. Reboot the module:
```
AT!RESET
```
   When the module reboots, the default state of GPIO6 is a digital input with a 10 µA pull-down function.

4.8.2 RESET_OUT_N

This pin can be used to provide a signal that will hold peripheral devices (such as a USB hub, I^2C device, etc.) in reset until the power-up sequence is complete.

To configure this pin as a Reset control signal:

1. Configure GPIO6:
```
AT+WIOCFG=6,0
```

   Note: For details, refer to [1] RC71xx AT Command Reference (Doc# 41114675).

2. Reboot the module.

When the module is:
- In reset or powering up — This pin is held low to put peripheral devices in reset. Once the power-on sequence is complete, this pin will be turned high to take the peripherals out of reset.
- In PSM — This pin will keep its previous status.

4.9 VGPIO

The Sierra Wireless RC71xx utilizes 1.8 V / 3.3 V logic, provided via the VGPIO (GPIO voltage output) pin.

Table 4-10: VGPIO Reference Pin

Pin	Signal Name	Direction[a]	Function	If Unused
45	VGPIO	Output	GPIO voltage output	Leave open

a. Signal direction with respect to the module — VGPIO (pin 45) is an output from the module to the host.

Table 4-11: VGPIO Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Remarks
Voltage level[a,b]	1.7	1.8	1.85	V	Supported when pin 145 (IO_VOL_SEL) is floating.
	3.2	3.3	3.35	V	Supported when pin 145 (IO_VOL_SEL) is connected to ground.
Current capability	–	–	50	mA	Power Management support up to 50 mA output

a. Voltage level applies to active mode and sleep mode.
b. The hardware setting of pin 145 (IO_VOL_SEL) must be fixed before boot-up. (i.e., Leave IO_VOL_SEL floating for 1.8 V, or connect to ground for 3.3 V)

The VGPIO voltage is available when the module is switched ON, and can be used to:

- Pull up signals such as I/Os
- Supply external digital transistors driving LEDs
- Supply external circuitry. Make sure you do not exceed the maximum current capability. Use an external regulator if a higher consumption is required.

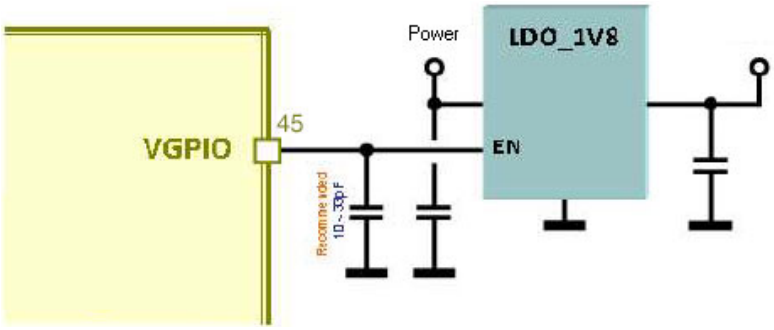


Figure 4-3: VGPIO connection to host platform

Note: VGPIO is at a high level (1.8 V or 3.3 V, dependent on pin 145 (IO_VOL_SEL)) when the module is in active or sleep mode. VGPIO is off (High-Z) when the module is in off mode.

4.10 Reset Signals (RESET_IN_N and RESET_OUT_N)

The Sierra Wireless RC71xx provides an interface to allow an external application to reset the module (RESET_IN_N) and reset the peripheral device (RESET_OUT_N).

Note: Using RESET_IN_N to reset the module could result in memory corruption if used inappropriately. This signal should only be used if the module has become unresponsive and it is not possible to perform a power cycle. Adding a test point is recommended.

Table 4-12: RESET Pins

Pin	Signal Name	Direction[a]	Function	If Unused
11	RESET_IN_N	Input	External Reset Input[b]	Leave open
46 (GPIO6)	RESET_OUT_N	Output	Peripheral devices reset	Leave open

a. Signal direction with respect to the module. e.g., RESET_IN_N (pin 11) is an input to the module from the host.
b. RESET_IN_N is a low-trigger signal. Module reset is triggered when input voltage < 0.38 V.

The RESET_IN_N signal is internally pulled-up with 170–230 kΩ (Note — Do not install an external pull-up on this pin). An open collector transistor or equivalent should be used to ground the signal when necessary to reset the module.

To reset the module, apply a low level pulse (< 0.38 V) on the RESET_IN_N pin. This will immediately restart the module.

The RESET_IN_N signal will reset the registers of the CPU and reset the RAM memory as well, for the next power on.

Table 4-13: Reset Timing

Symbol	Parameter	Min	Typ	Unit
Trdet	Duration of RESET_IN_N signal before firmware detects it (debounce timer)	—	350	µs
Trlen1	Duration RESET_IN_N asserted	—	450	ms
Trlen2	Duration RESET_OUT_N asserted	420	—	ms

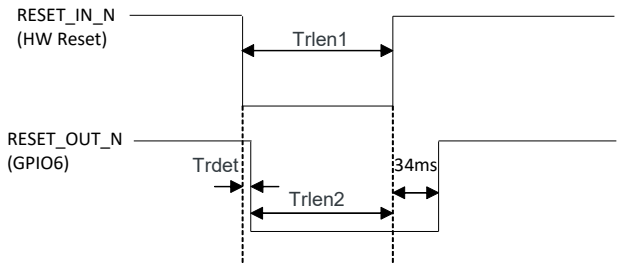


Figure 4-4: Reset timing

4.11 ADC

The Sierra Wireless RC71xx provides two general purpose ADC (Analog to Digital Converter) inputs, as described in Table 4-14 and Table 4-15.

Table 4-14: ADC Interface Pins

Pin	Signal Name	Direction[a]	Function	If Unused
24	ADC1	Input	Analog to Digital Converter	Leave open or Ground
25	ADC0	Input	Analog to Digital Converter	Leave open or Ground

a. Signal direction with respect to the module. Example: ADC1 (pin 24) is an input to the module from the host.

Table 4-15: ADC Interface Characteristics

Parameter	Value	Units
Full-scale voltage level	0–1.2	V
Resolution	12	bit
Sample rate	Clock rate: 1.625 ~ 6.5 (Typ = 3.25)	MHz
	Sampling rate: 101 ~ 406 (Typ = 203)	KHz
Voltage error	7 (Typ); 14 (Max)	mV

4.12 TP1 (Boot Pin)

The TP1 pin (boot pin) can be used for two primary purposes:

- Install full firmware updates via the USB Serial COM port by placing the module in bootloader mode (Note — This is not required for delta firmware updates.)

  Full firmware updates can only be performed when the module is in bootloader mode.

  To install a full firmware update using the TP1 pin:

  i. Connect TP1 to a control mechanism (e.g., a button, switch, or jumper) on the host platform.

  ii. Activate the control mechanism to drive (assert) TP1 low and keep it low — e.g., press and hold the button, toggle the switch, close the jumper, etc.

  iii. While TP1 is being asserted (kept low), restart the module using an appropriate method, such as:
  - Use the RESET_IN_N pin as described in Reset Signals (RESET_IN_N and RESET_OUT_N).
    (Note — The RESET_OUT_N pin is an output from the module that indicates a RESET has been performed.)
  - Use POWER_ON_N as described in POWER_ON_N.
  - If the module is currently powered on, use the command **AT!RESET**.

  When the module starts to power up, the bootloader process detects that TP1 is low, stops the power on process, and begins to download a full firmware update via the USB Serial COM port.

  iv. After the download starts, deassert TP1. (This will allow the module to boot normally after the download finishes.)

  v. Wait for the download to finish. When it finishes, the module reboots automatically. If TP1 was deasserted (in step iv), the module boots normally with the new firmware.

- RMA debugging by Sierra Wireless
  TP1 must remain acessible on the host platform for use by Sierra Wireless in RMA debugging.

Note: Firmware downloads also occur using software tools available at source.sierrawireless.com.

Table 4-16: TP1 Pin Description

Pin	Name	Direction	Function	Note
47	TP1	Input	Device recovery (boot load): ▪ 0 — Enter download mode ▪ Open — Normal mode	TP1 should remain accessible for use by Sierra Wireless in RMA debugging.

4.13 Test Points

Test points are recommended on several pins (Table 4-17). Note — Sierra Wireless requires test points on the customer application for RMA and debug service.

Table 4-17: Recommended Test Points

Pin	Name	Function	If interface / signal is unused
Control signals			
11	RESET_IN_N	Control signal	A test point is strongly recommended for use as a hardware reset.
46	GPIO6/RESET_OUT_N	GPIO/Control signal	Recommended
47	TP1 (Boot pin)	Control Signal	A test point is strongly recommended for emergency downloads Use TP1 to initiate full firmware downloads: ▪ 0 (asserted) — Enter Download mode ▪ Open (floating) — Normal mode
59	POWER_ON_N	Control Signal	A test point is strongly recommended for debug purposes.
151	W_DISABLE_N	Control Signal	Recommended
Voltage reference			
45	VGPIO	Voltage reference	A test point is strongly recommended for debug purposes.
UART			
3	UART1_RTS	UART1	Test points are strongly recommended for debug purposes.
4	UART1_CTS		
5	UART1_TX		
6	UART1_RX		
96	UART2_TX	UART2	
97	UART2_RX		
98	UART2_RTS		
99	UART2_CTS		

Table 4-17: Recommended Test Points (Continued)

Pin	Name	Function	If interface / signal is unused
USB			
12	USB_D-	USB	Test points are strongly recommended for debug purposes.
13	USB_D+	USB	
16	USB_VBUS	USB	
UIM			
26	UIM1_VCC	UIM1	Recommended
27	UIM1_CLK	UIM1	
28	UIM1_DATA	UIM1	
29	UIM1_RESET_N	UIM1	
64	UIM1_DET	UIM1	
65	UIM2_DET/GPIO4	UIM2	

4.14 Antenna Control

The Sierra Wireless RC71xx provides four output signals that can be used for host designs that incorporate a tunable antenna.

Note:

- *It is the responsibility of developers of host designs to evaluate the performance of tunable antennas that use these signals for neighbor cell measurements, Inter-RAT handovers, etc. Sierra Wireless does not guarantee ANT_CNTLx signal timing.*
- *Antenna control signals support is optional.*

Table 4-18: Antenna Control Signals

Pin	Name	Direction[a]	Function	If Unused
153	ANT_CNTL0	Output	Customer-defined external switch control for tunable antenna	Leave open
154	ANT_CNTL1	Output		Leave open

a. Signal direction with respect to module. Examples: ANT_CNTL0 (pin 153) is an output from the module to the host.

To tune the antenna:

1. Enable band selection, which is required to tune the antenna for specific bands:
   ```
   AT!CUSTOM="BANDSELEN",1
   ```
   Note that this setting is persistent unless disabled by issuing
   ```
   AT!CUSTOM="BANDSELEN",0
   ```

2. Drive the antenna control signals high or low, as required, for a specific band:
   ```
   AT!ANTSEL=<band>, <gpio1>, <gpio2>
   ```
   Refer to *[1] RC71xx AT Command Reference (Doc# 41114675)* for details.
   Note that <gpio1>–<gpio2> correspond to ANT_CTRL0–ANTCTRL1.

4.15 Indication Interfaces

The Sierra Wireless RC71xx provides several indication interfaces that deliver notifications when specific events occur. These interfaces include:

- WWAN_LED_N
- WAKE_ON_WWAN
- Ring Indicator
- SAFE_PWR_REMOVE

4.15.1 WWAN_LED_N

The Sierra Wireless RC71xx provides an LED control output signal pad.

Table 4-19: LED Interface Pin

Pin	Signal Name	Direction	Voltage / Current	Function	If Unused
106	WWAN_LED_N	Output	▪ Voltage (max) = Typical output range: ▪ (VGPIO = 1.8V) 0.3–1.8 V ▪ (VGPIO = 3.3V) 0.5–3.3V	LED driver control	Leave open

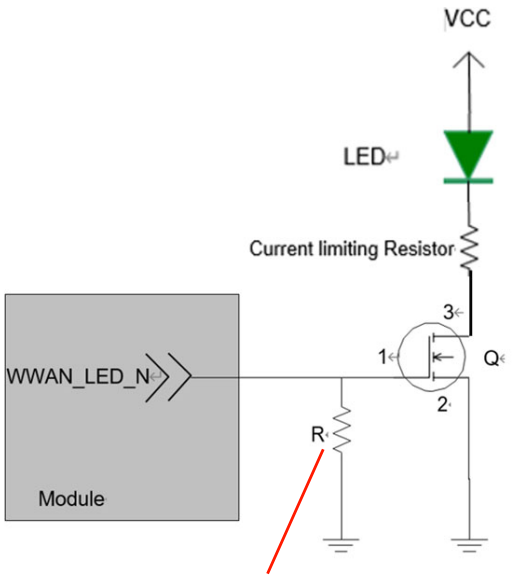


Figure 4-5: Recommended WWAN_LED_N Connection

4.15.2 WAKE_ON_WWAN

Note: Host support for WAKE_ON_WWAN signal is optional.

The Sierra Wireless RC71xx drives WAKE_ON_WWAN high to wake the host when specific events occur.

See Figure 4-6 for a recommended implementation.

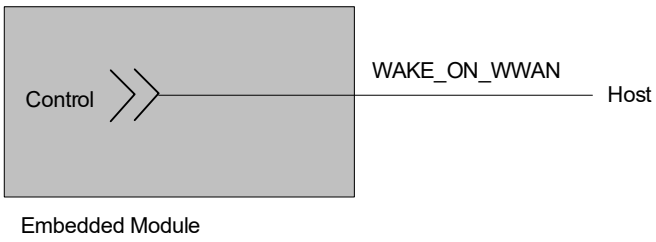


Figure 4-6: Recommended WAKE_ON_WWAN Connection

Note: Pin status is in internal pull-down when the module boots or resets.

4.15.3 Ring Indicator

The ring indicator (UART1_RI) may be used to notify an external application of several events such as an incoming call, timer expiration, or incoming SMS. The Sierra Wireless RC71xx pulses the signal low when an event occurs. It can be used independently from the UART1 interface.

Table 4-20: UART1_RI (Ring Indicator) Timing Parameters

Parameter	Time
Pulse width	50 ms

*Note: The pulse width duration is based on the current FW setting and can be configured using the AT command: **AT+WRID**.*

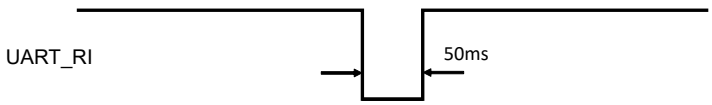


Figure 4-7: UART1_RI (Ring Indicator)

Table 4-21: UART1_RI Pin

Pin	Name	Direction[a]	Function	If unused
2	UART1_RI	Output	▪ Ring Indicator ▪ Signal incoming calls, SMS, etc.	Leave open

a. Signal direction with respect to the module — UART1_RI (pin 2) is an output from the module to the host.

Important: *Do not install an external pull-up on this pin, otherwise the module will not boot.*

Note: Pin status is in internal pull-down when the module boots or resets.

4.15.4 SAFE_PWR_REMOVE

The SAFE_PWR_REMOVE signal is provided by the RC71xx to indicate to the host device that the main power supply (VBATT) can be safely turned off after a positive pulse.

Table 4-22: SAFE_PWR_REMOVE Timing Parameters

Parameter	Value
Pulse width	13 ms
SAFE_PWR_REMOVE falling edge to VPGIO off	1 s

Note:
- *All host interfaces connected to the module must be disabled (High-Z or pull-down) before turning off VBATT. This prevents leakages and bad power on sequences.*
- *Consider the VGPIO discharge time (depends on the load on the host equipment) before switching off VBATT.*

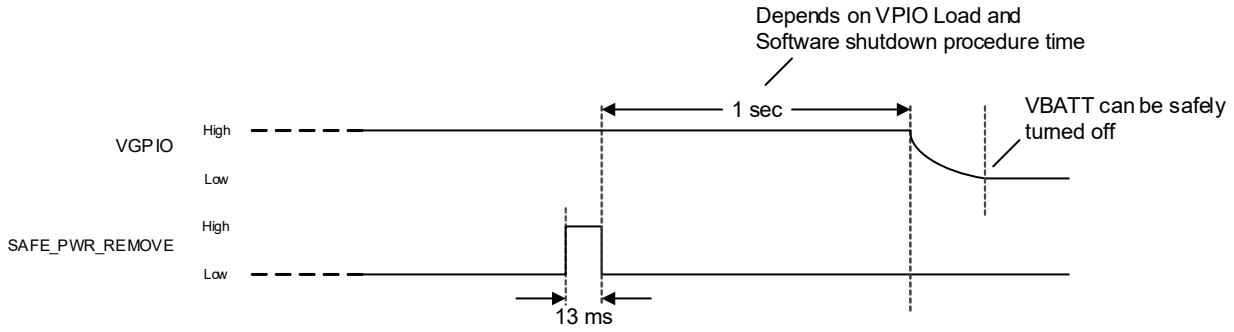


Figure 4-8: SAFE_PWR_REMOVE

4.16 W_DISABLE_N — Wireless Disable

Note: Host support for wireless disable signals is optional.

The host device uses W_DISABLE_N (pin 151) to enable/disable the WWAN or radio modem. When disabled, the modem cannot transmit or receive information.

Letting this signal float high allows the module to operate normally. The pin has an internal pull-up resistor. See Figure 4-9 for a recommended implementation.

When integrating with your host device, keep the following in mind:

- The signal is an input to the module and should be driven LOW only for its active state (controlling the power state), otherwise it should be floating (or High-Z). It should never be driven to a logic high level. The module has an internal pull-up resistor to an internal VGPIO power rail, so if the signal is floating (or High-Z), then the radio is on.
- If the host never needs to assert this power state control to the module, leave this signal unconnected from the host interface.

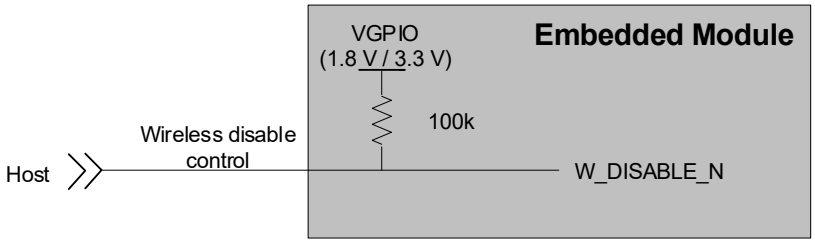


Figure 4-9: Recommended Wireless Disable Connection

5: Routing Constraints and Recommendations

This section describes general routing constraints and recommendations for the Sierra Wireless RC71xx module.

Note: This is a non-exhaustive list of suggested design guidelines. The developer is responsible for deciding whether to implement these guidelines.

5.1 General Rules and Recommendations

Clock and other high-frequency digital signals (e.g., serial buses) should be routed as far as possible from the module's analog signals.

If the application design makes it possible, all analog signals should be separated from digital signals by a ground trace on the PCB.

Note: Avoid routing any signals under the module on the application board.

5.2 Power Supply

When designing the power supply, make sure that VBAT_BB/VBAT_RF meet the requirements listed in Power Supply Ratings.

Careful attention should be paid to the following:

- Power supply noise — PFM systems should be avoided; Low ripple, linear regulation or PWM converters are preferred for low noise.
- High switching load capability to deliver high current peaks in a short time. For details about the input capacitor, see Power Supply.
- Power supply and power traces design must support peak currents with an acceptable voltage drop that guarantees the minimum required VBATT value.
- Voltage applied on VBATT signal pads must never exceed the voltage range defined in Power Supply Ratings, otherwise the module's power amplifier may be severely damaged.
- A weakly-designed (not robust) power supply could affect EMC performance, the radiated spurious emission (RSE), and the phase error and frequency error.

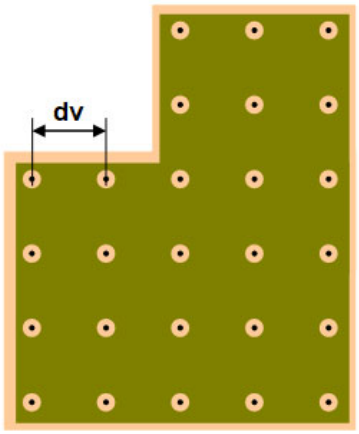
5.3 PCB Layout Recommendations

5.3.1 General Design Rules

- Application board should be designed in such a way that provides a plain GND connection on the whole surface located under the module area. A matrix of high density vias should be implemented to connect the top layer (in contact to the module LGA ground pads) to other GND layers. Such implementation aims to reduce noise interference, spurious radiation and improve heat dissipation spreading heat through the PCB surface and layers.
- To reduce coupling between antenna and other signals and improve EMC, the top and bottom layers of the PCB should be covered by solid GND plane as much as possible.

- Good PCB grounding is essential; use GND planes that are as wide as possible and link the different GND planes from each layer using regularly spaced via holes.

  The maximum recommended distance between two consecutive vias is calculated as shown in the following example:



The "dv" distance between two GND vias should be calculated using the empirical equation below:

$$dv \leq \frac{1}{10} \cdot \frac{\lambda g}{4} = \frac{1}{40} \cdot \lambda g$$

With $\lambda g = \frac{c}{F\max \cdot \sqrt{\varepsilon_r}}$

c = velocity of light $\approx 300.10^9$ mm/s

Fmax = Highest frequency used on the application

ε_r = relative permittivity (dielectric constant) of PCB

So for a 2GHz / FR4 application, dv should be :

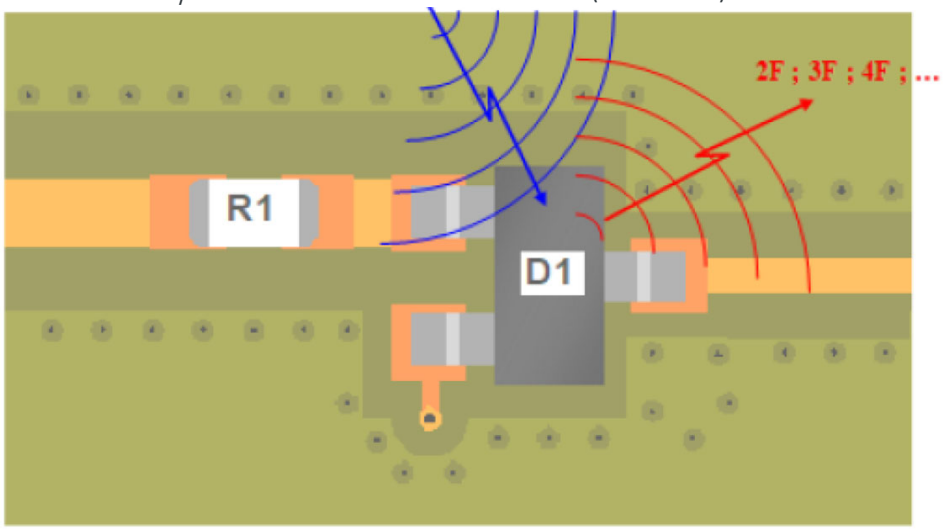
$$dv_{2,7GHz/FR4} = \frac{1}{40} \cdot \frac{300}{2,7 \cdot \sqrt{4,6}} \approx 1,3mm$$

- Particularly, via should be present all around the PCB edge to block any unwanted EMI emitted from the internal layers. Usually power planes are not recommended. We recommend a distributed power supply instead.

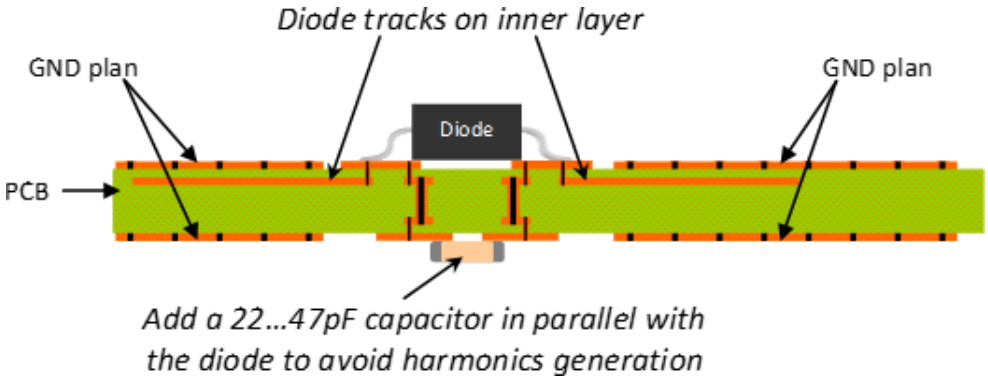
- Sensitive signals should be shielded by routing them into inner layers (to prevent them from radiating) and sensitive components can be shielded. The top and bottom ground planes connected together with vias ensures all sensitive traces are shielded well. This significantly reduces coupling between antenna and other signals and improves EMI and EMC performances.
- When it is not possible to route a signal trace into inner layers, top and bottom layers can be used for short distance connections (i.e., connections between adjacent pads).
- It is good practice during the design phase to anticipate and reserve area for shield cans.
- The module's power supply needs decoupling capacitors to filter out noise to prevent it from reaching the module. It could cause instabilities in the RF output in the transmitter, resulting in undesired interference and spurious radiations. In the receiver, it increases packet error and reduces sensitivity.
- Place a decoupling capacitor (10–33 pF is recommended) as close to the power supply pin of the module as possible.
- Use as many vias as possible to build a ground fence around the RF stripline and microstrip line to isolate it from other signals.
- In some specific cases, like impedance controlled lines and RF connection pads and antenna pads, sufficient keep out distance between RF signals and GND should be implemented to prevent impedance mismatch from parasitic capacitance load.

5.3.2 Specific Design Rules to Support TRP Performance

- Prevent interference between neighboring components caused by TX radiated RF energy, to prevent the components from generating harmonics through non-linear behavior such as saturation or rectification. If the host platform design does not prevent this interference, it may easily fail to meet the R&TTE/PTCRB certification mandatory maximum radiated harmonics level (< -30 dBm).



- For example, when possible, add 10-47pF in parallel of each fast rectifier diode to prevent generating harmonics (due to the TX signal detection).



- With an antenna located close to circuitry using active devices, shielding may be needed to reach enough isolation.

5.3.3 Specific Design Rules to Support TIS Performance

- High speed digital signals (e.g., DC/DC converters, system clock, CPU and Memory bus, USB and other high-speed interfaces) should be routed on inner layers and located as far as possible from RF signals and antenna.
- Good practice for interference prevention is to add decoupling capacitors (10–33 pF recommended) every 10 mm on all top and bottom power lines longer than 10 mm.
- With an antenna located close to circuitry using active devices or noisy signals, shielding may be needed to reach enough isolation.

5.4 PCB Specifications for the Application Board

Digital and sensitive signals (such as audio, UIM, clocks, high speed interface) should be routed on the inner layers and separated from each other by GND traces regularly punctured with vias (or microvias). Routing sensitive signals close to noisy signals could result in noise being coupled.

5.5 Recommended PCB Land Pattern

Refer to document *[2] RC71xx Customer Process Guidelines (Doc# 41114682)*, available at source.sierrawireless.com.

5.6 Routing Constraints

5.6.1 Power Supply

Note: The recommended output current rating for the power supply on Table 3-3 on page 18 includes margin.

If the following design recommendations are not followed, phase error (peak) and power loss could occur.

- The trace widths of the power supplies (VBAT_BB and VBAT_RF) should be as wide as possible (> 1.5 mm) to minimize voltage drops and reduce electromagnetic interference risks.

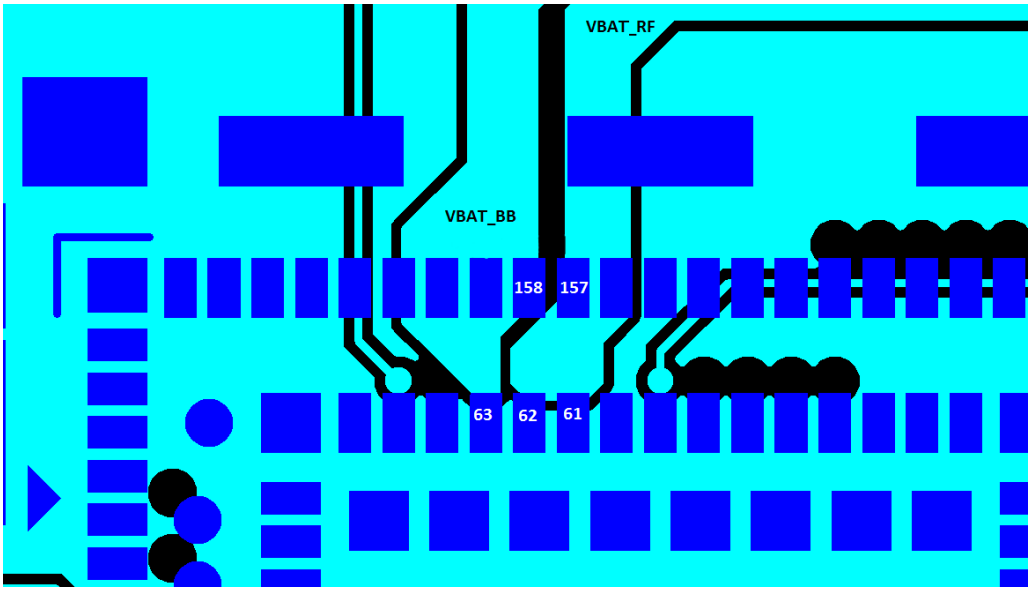


Figure 5-1: Power Supply Routing Example

Note: Figure 5-1 shows separate traces for VBAT_BB and VBAT_RF. If VBAT_BB and VBAT_RF share a single power supply, these traces should be connected.

Note: For optimal decoupling, place the capacitors on the underside of the board, directly under the pins.

- Reserve space for capacitors close to the module — depending on the quality and stability of the power supply, either:
  - at least two capacitors (> 47 µF)
    or
  - 1×47 µF+ 2×22 µFcapacitors
- Attention should be paid to the ground trace or the ground plane on the application board for the power supply that supplies the module. The ground trace or ground plane, as well as the VBATT trace, must be able to support current peaks.
- If the ground trace between the module and the power supply is a copper plane, make sure it is a solid plane.
- Design routing to make sure total line impedance does not exceed 10 mΩ.

5.6.1.1 Ground Plane Connection

The Sierra Wireless RC71xx requires a solid, central ground plane (with solder mask defined pads) located directly under the module. This will:

- Ensure high current signal returns
- Provide heat dissipation under higher operating temperatures

The ground plane should be connected (with vias) to the reference ground layer of the application board.

Do not use a separate GND for the antenna. Connections to GND from the Sierra Wireless RC71xx module should be flooded plane using thermal reliefs to ensure reliable solder joints.

5.6.2 UIM Interface

- Traces between the module and the UIM socket should be as short as possible and routed on inner layers. Maximum recommended length is 10 cm.
- The ESD must be placed near the UIM holder
- ESD protection is mandatory on the UIM lines unless there is no physical access to the UIM.
- The decoupling capacitor(s) should be placed as close as possible to the UIM card connector for the UIM1_VCC and UIM2_VCC signals.
- Isolate UIM1_CLK/UIM2_CLK and UIM1_DATA/UIM2_DATA from other signals and from each other.

  Close routing between each UIM's Clock and Data signals is not recommended — Sierra Wireless recommends:
  - 2x spacing between UIM1_CLK and UIM1_DATA
  - 2x spacing between UIM2_CLK and UIM2_DATA
  - 50 Ω impedance control

5.6.3 RF Routing Recommendations

To reduce potential performance issues, Sierra Wireless strongly recommends the following RF routing layout guidelines be considered on the PCB layout:

- The antenna interface (RF_MAIN) and related GND pads should be considered as an integrated part of the radio input/output (see Figure 5-4).

  The reference ground of the RF traces must be a solid integrated plane.
- The use of a CBCPW (Conductor-Backed Coplanar Waveguide) is strongly recommended for lower insertion loss, better impedance matching stability and no additional loss due to the use of vias required by the Stripline structure.

The CBCPW must be surrounded by GND planes evenly punched by GND vias:

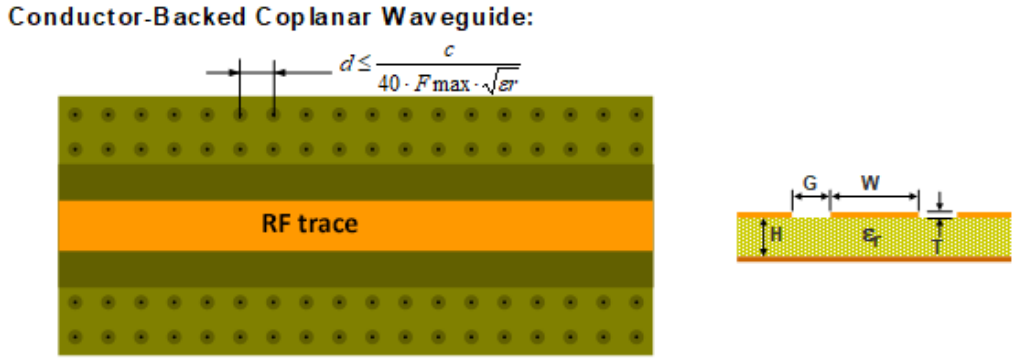


Figure 5-2: Conductor-Backed Coplanar Waveguide (CBCPW) design

- The distance between two adjacent vias should be ≤ the quarter wavelength / 10 of the highest frequency carrier.
- The CBCPW design for RF trace must be used for better isolation, and the coplanar clearance (G, below) from the trace to the ground should be at least the trace width (W) and at least twice the height (H). This reduces the parasitic capacitance, which potentially alters the trace impedance and increases the losses.

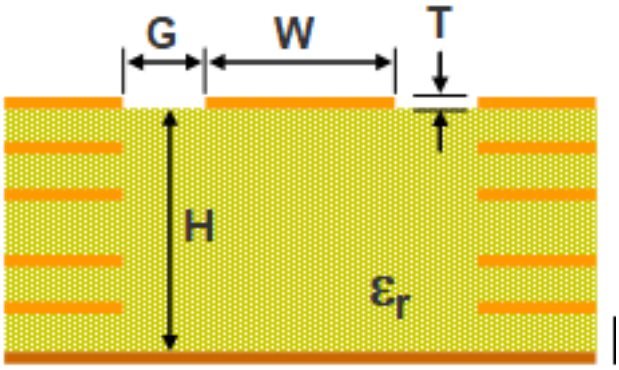


Figure 5-3: Coplanar Clearance example

Note: The figure above shows several internal ground layers cut out, which may not be necessary for every application.

- As far as possible and in order to avoid impedance breaks, choose an RF trace width at least equal size of the component pad connected to it.

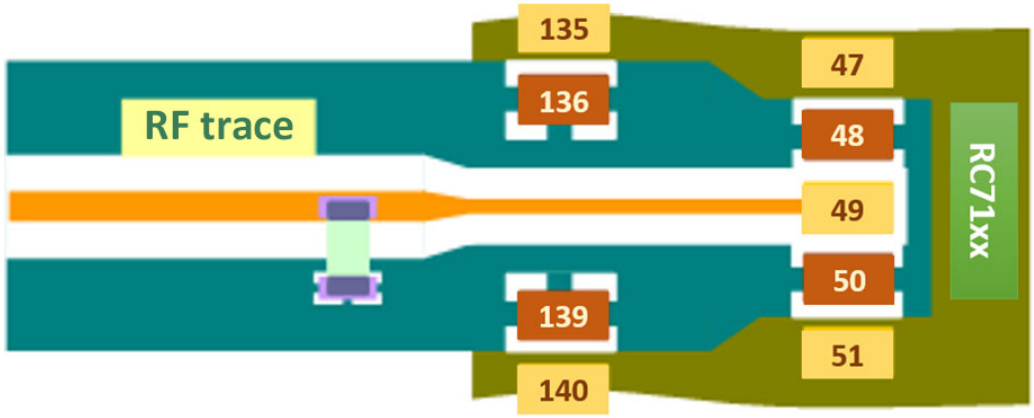


Figure 5-4: Trace width and component pad

- RF traces must be routed with well-controlled 50 Ω single-ended lines (microstrip or stripline) and have a solid ground.
  As shown in Figure 5-4, part of the RF trace is routed under the module. To account for the metallic mass of the module, the RF trace width may need to be slightly reduced before going under the module. Thus, under the module, the structure of the RF line becomes a stripline.
- Include a copper keep-out under the RF pads to reduce stray capacitance losses.

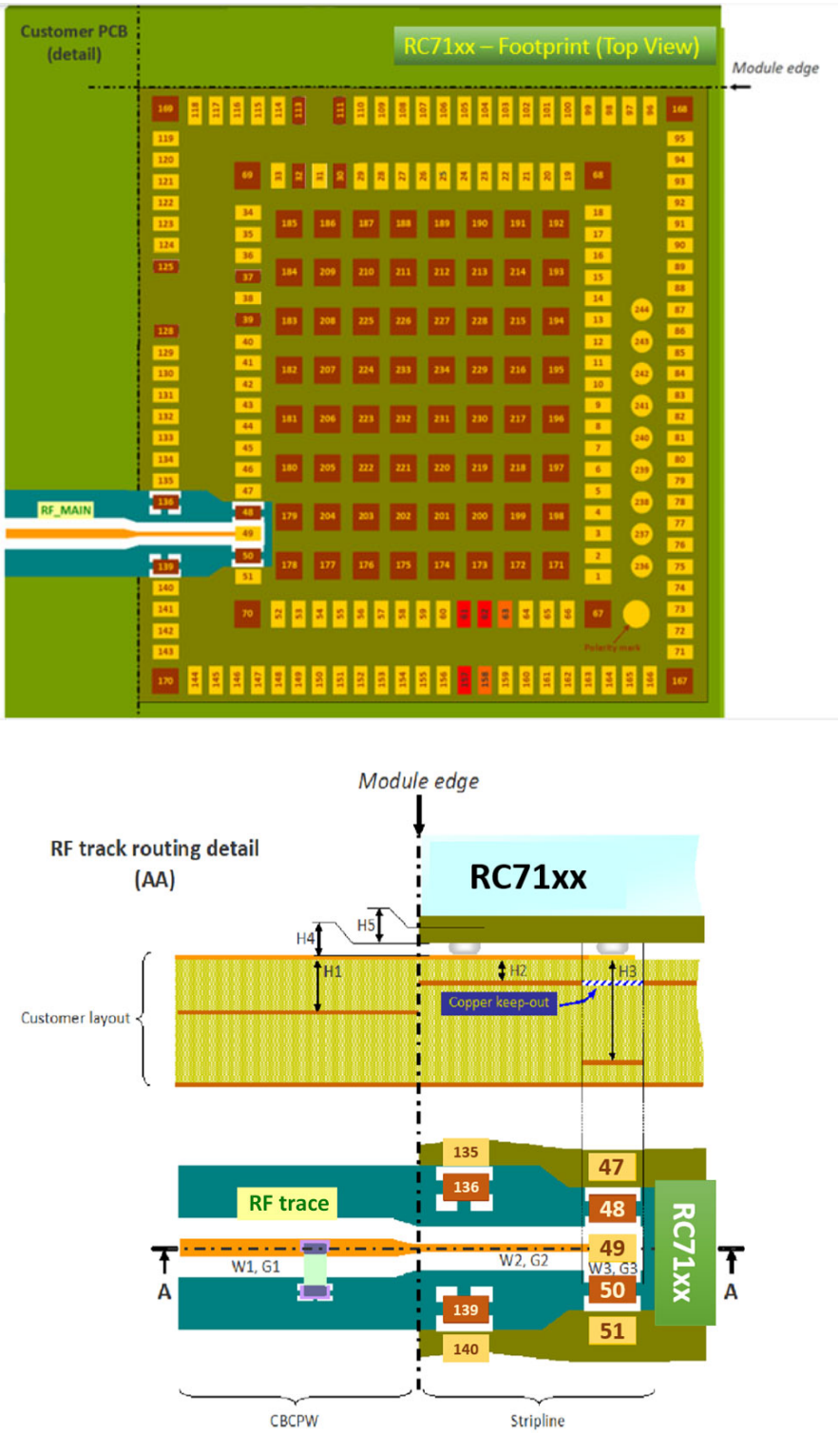


Figure 5-5: RF Traces Routing

- All RF traces must be well-isolated from other noisy circuits such as switching power supply, clock and antenna control signals, and sensitive functions and traces. Make sure the signal is not susceptible to interference and does not interfer with other signals.
- Edge mount RF connectors are strongly suggested for better impedance matching.

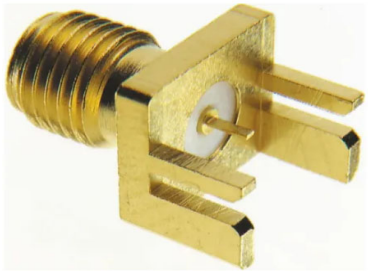


Figure 5-6: RF Connector

- When designing PCB traces, avoid routing designs that use different layers with via transitions, since this may introduce additional RF losses and path inductance.
- Do not use right angle RF traces. A 90^{o} mitered bend is recommended:

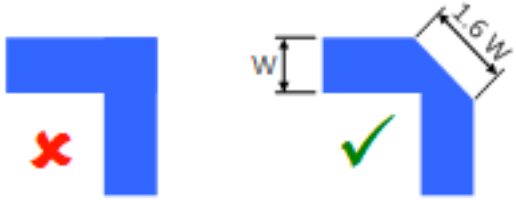


Figure 5-7: RF traces — Example of optimally 90^{o} mitered bend routing

5.6.4 USB Interface

When the USB interface is externally accessible, ESD protection is required on the USB_VBUS, USB_D+, and USB_D- signals.

HS-USB guidelines:

- Up to 480 Mbps data rate.
- 90 Ω differential, ± 10% trace impedance.
- Differential data pair matching < 3.8 mm (150 mils).
- Other comments and guidelines:
  - External components should be located near the USB connector.
  - Relatively fast edge rates, so they should be routed away from sensitive circuits and signals (RF, system clock).
  - VBUS trace width must be sized depending on the length of VBUS and the expected current.
  - Loading on the USB DP/DM lines could cause USB receiver sensitivity issues. Perform USB electrical tests (eye diagram and receiver sensitivity) to ensure proper USB functionality.
  - It is not recommended to install series switches on the USB lines.
  - Trace width and trace spacing for DP and DM based on impedance calculator. Avoid discontinuity. The trace width should be equal from source to destination. Keep impedance constant.
  - Avoid having multiple vias. Vias are a source of discontinuity, which can cause signal reflection.
  - Avoid crossing different power planes if possible for USB signals. This causes an unpredictable return path current and causes a signal quality issue.

- Avoid stubs. A common routing mistake is to create a stub by connecting a component on the DP or DM traces.
- Test points added on USB traces must comply with radio frequency signal routing rules to avoid degradation of USB signal quality.
- The USB power supplies should have wider traces and not narrow traces, which cause IR drop. This affects the jitter performance of the USB signal.

5.7 EMC and ESD Recommendations

EMC tests must be performed on the application as soon as possible to detect any potential problems.

When designing, special attention should be paid to:

- Possible spurious emissions radiated by the application to the RF receiver in the receiver band
- ESD protection — Typically, ESD protection is mandatory for externally accessible signals, including:
  - VBAT_RF/VBAT_BB
  - UIM (if accessible from outside)
  - Serial link
  - USB
  - Antenna
  - Key Feature (Control signals)
- Length of the UIM interface lines (preferably <10 cm)
- Ground plane: Sierra Wireless recommends a common ground plane for analog/digital/RF grounds.

Note: The Sierra Wireless RC71xx does not include any protection against over-voltage.

The host device must provide adequate ESD protection on digital circuits and antenna ports as detailed in Table 5-1.

Note: The level of protection required depends on your application.

Table 5-1: ESD Specifications[a]

Category	Connection	Specification
Operational	▪ RF ports ▪ UIM connector ▪ USB connector ▪ UART connector	IEC-61000-4-2 - Level (Electrostatic Discharge Immunity Test) ▪ ± 6kV Contact ▪ ± 8kV Air
Non-operational	Host connector interface	Unless otherwise specified: ▪ JESD22-A114 ± 1kV Human Body Model ▪ JESD22-A115 ± 100V Machine Model ▪ JESD22-C101C ± 500V Charged Device Model

a. ESD protection is highly recommended at the point where the UIM contacts are exposed, and for any other signals that would be subjected to ESD by the user.

5.8 Mechanical Integration

Attention should be paid to:

- Antenna cable integration (bending, length, position, etc)
- Pads of the Sierra Wireless RC71xx to be soldered to the ground plane
- Ensuring proper board layout
- Providing sufficient space around the module for heat dissipation

5.9 Signal Reference Schematics

5.9.1 UIM Holder

Figure 5-8 illustrates the recommended implementation of a UIM holder (i.e., for UIM1 or UIM2).

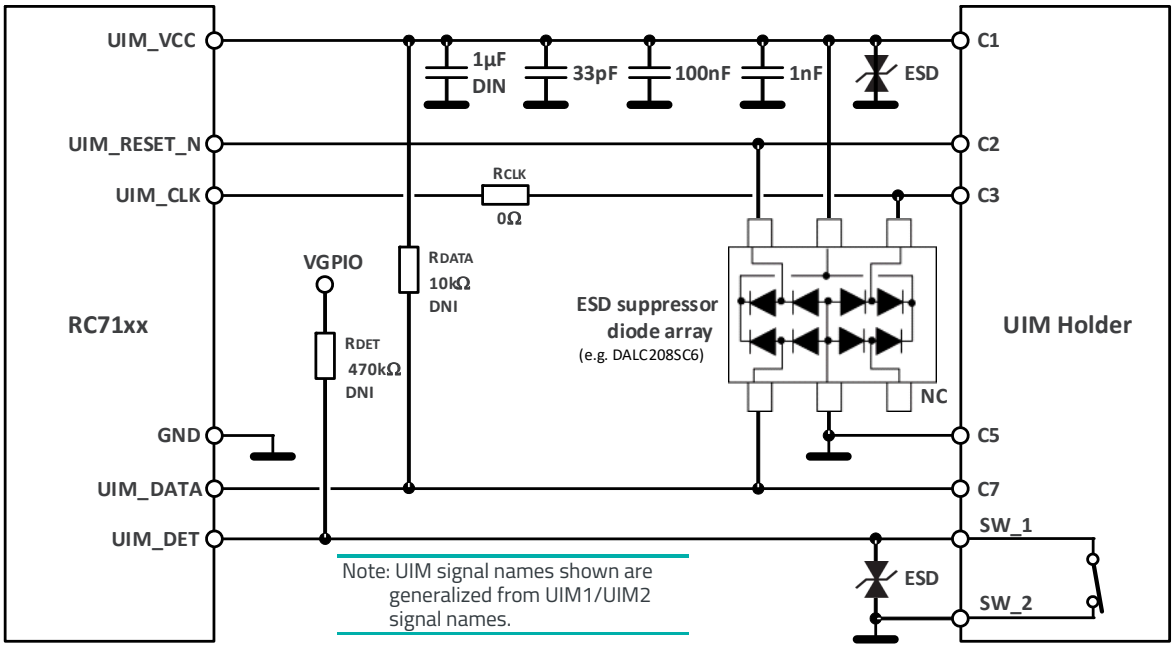


Figure 5-8: Recommended UIM Holder Implementation for UIM1 and UIM2

The UIM Detect signals (UIM1_DET, UIM2_DET) is used to detect the physical presence of a UIM card in the UIM holder. The signal has a 470 kΩ pull-up internal to the module. It should be set to GND when a UIM is not present. The UIM Detect signal transitions:

- When a UIM is inserted — high (logic 0 to logic 1)
- When a UIM is removed — low (logic 1 to logic 0)

Recommendations:

- The capacitor and the two resistors (RCLK, RDATA) should be added as placeholders to compensate for potential layout issues.
- UIM data (UIM1_DATA, UIM2_DATA) traces should be routed away from the UIM clock (UIM1_CLK, UIM2_CLK) traces.
- Keep the distance between the module and the UIM holder as short as possible.
- All signals near the UIM holder must be ESD-protected.

- An ESD device specifically designed for UIM cards is recommended for the VCC (UIM1_VCC. UIM2_VCC), Reset (UIM1_RESET_N, UIM2_RESET_N), Clock (UIM1_CLK, UIM2_CLK), and data (UIM1_DATA, UIM2_DATA) signals (for example, STMicroelectronics DALC208SC6).

  Low leakage ESD suppressors should be selected for the UIM Detect signals (UIM1_DET, UIM2_DET).

5.9.2 USB

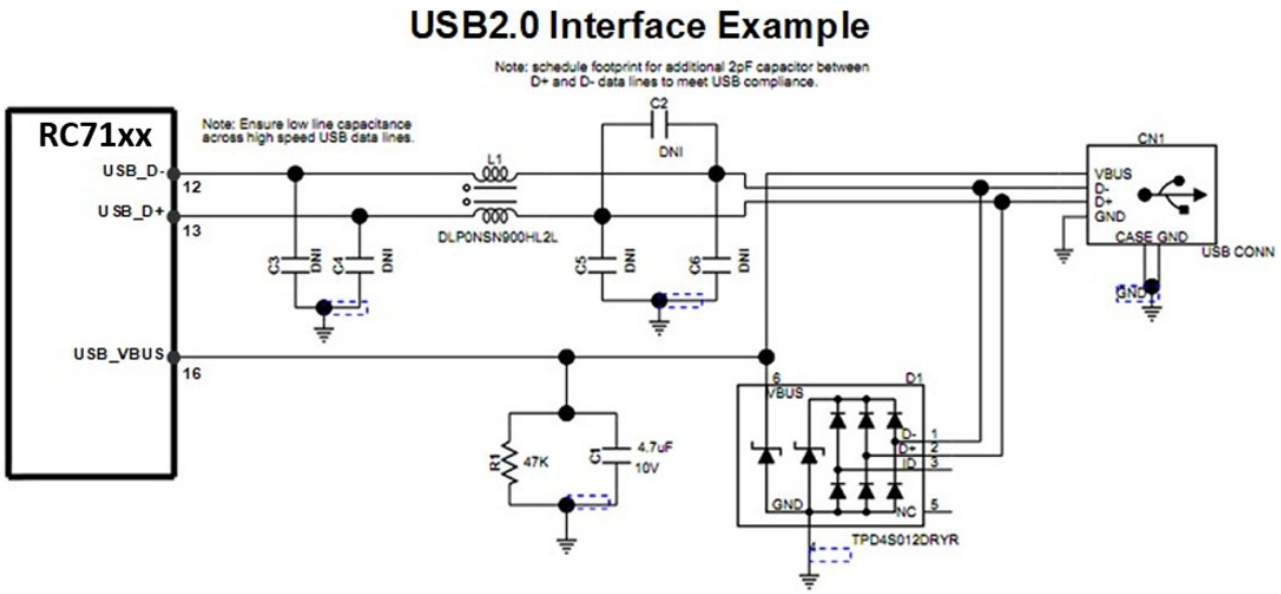


Figure 5-9: USB Interface

5.10 Thermal Considerations

When transmitting, the RC71xx can generate significant amounts of heat (due to the internal Power Amplifier) that must be dissipated in the host device for safety and performance reasons.

The amount of thermal dissipation required depends on the following factors:

- Supply voltage — Maximum power dissipation for these modules can be up to 2.85 W at voltage supply limits.
- Usage — Typical power dissipation values depend on the location within the host, amount of data transferred, etc.

To enhance heat dissipation:

- Maximize airflow over / around the module
- Locate the module away from other components that generate heat
- Ensure the module is connected to a solid ground plane.

6: Debug and Assembly Considerations

6.1 Integration Requirements

When integrating the Sierra Wireless RC71xx, the following items must be addressed:

- Mounting — Effect on temperature, shock, and vibration performance
- Power supply — Impact on battery drain and possible RF interference
- Antenna location and type — Impact on RF performance
- Regulatory approvals — As described in Regulatory Compliance and Industry Certifications
- Service provisioning — Manufacturing process

For board mounting design guidelines, refer to *[2] RC71xx Customer Process Guidelines (Doc# 41114682)*. For integration support, please contact your Sierra Wireless technical support representive.

6.2 IOT / Operator

Interoperability and Operator/Carrier testing of the finished system is the responsibility of the OEM. The test process will be determined with the chosen network operator(s) and will be dependent upon your business relationship with them, as well as the product's application and sales channel strategy.

Sierra Wireless offers assistance to OEMs with the testing process, if required.

6.3 Module Testing Recommendations

When testing your integration design:

- Test to your worst case operating environment conditions (temperature and voltage)
- Test using worst case operation (transmitter on 100% duty cycle, maximum power)
- Monitor the module's junction temperature using **AT!PATEMP**. This command polls a thermistor located near the module's power amplifier (typically the hottest spot on the module).

Note: Make sure that your system design provides sufficient cooling for the integrated module. The RF shield temperature should not be exposed to an ambient temperature greater than 85 °C to prevent damage to the module's components.

6.4 Serial Link Access

Direct access to the UART1 serial link is very useful for:

- Testability operations
- Accessing the module's console for debugging

Refer to the following figure for a level shifter implementation that allows UART1 serial link access.

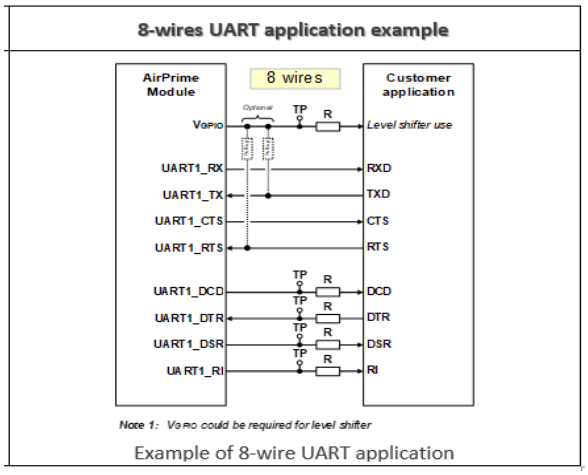


Figure 6-1: UART Application sample (Module level = 1.8 V)

6.5 RF Output Accessibility

During the integration phase of the Sierra Wireless RC71xx, it can be helpful to connect the module to a simulator to check critical RF TX parameters and power behavior for supported RATs.

Although the module has been certified, some parameters may have degraded if some basic precautions have not been followed (poor power supply, for example). This may not affect the functionality of the product, but the product may not comply with 3GPP specifications.

The following TX parameters can be checked using a Radio Communication tester (e.g., Rohde & Schwarz CMW500, Anritsu MT8821C, etc.):

- Phase & Frequency Error
- Output Power and Burst Time
- Output Spectrum (Modulation and Switching)

6.6 USB Debug

The USB interface is also used to collect traces for debug purposes. It is highly recommended to reserve test points for collecting traces when USB is not used. Refer to USB for additional interface description.

7: Reliability Specification

7.1 Functional / Performance Tests

- Operating Condition: Powered
- Test Temperature: Class A and Class B

7.2 Aging Tests

7.2.1 High Temperature Operating Life Test

- Standard: IEC 60068-2-2, Test B: Dry heat
- Test Temperature: 85°C
- Operating Condition: 45 minutes Max Tx/15 minutes Idle
- Duration: 20 days

7.2.2 Humidity Test

- Standard: IEC 60068-2-78, Test Cab: Damp heat, steady state
- Test Temperature: 70°C
- Relative Humidity: 95%
- Operating Condition: 15 minutes Idle/15 minutes Off
- Duration: 20 days

7.2.3 Thermal Shock Test

- Standard: IEC 60068-2-14, Test N: Change of temperature
- Test Temperature: -40°C to 85°C
- Temperature Transition Time: < 30 seconds
- Dwell Time: 10 minutes
- Operating Condition: Unpowered
- Duration: 300 cycles

7.3 Characterization Tests

7.3.1 Electrostatic Discharge Test

- Standard: IEC 61000-4-2: Testing and measurement techniques — Electrostatic discharge Immunity test
- Operating Condition: Powered
- Air Voltage: ±2kV, ±4kV, ±8kV
- Contact Voltage: ±2kV, ±4kV, ±6kV

7.3.2 Low Temperature Cold Start Test

- Standard: IEC 60068-2-1, Test A: Cold
- Test Temperature: -40°C
- Operating Condition: 30 minutes Off/5 minutes Idle
- Duration: 5 days

7.3.3 Electrostatic Discharge Component Test

- Standard: ANSI/ESDA/JEDEC JS-001, ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM) — Component Level
- Standard: ANSI/ESDA/JEDEC JS-002, ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Charged Device Model (CDM) — Device Level
- CDM: 500 V
- HBM: 2000 V
- Operating Condition: Powered

7.3.4 Unprotected Free Fall Drop Test

- Standard: IEC 60068-2-31, Test Ec: Rough handling shocks, primarily for equipment-type specimens
- Number of Drops: 1 drop per direction (±X, ±Y, ±Z), 6 directions
- Surface Type: Un-protected drops onto concrete
- Drop Height: 1 meter
- Operating Condition: Unpowered

7.3.5 Component Solderability Test

- Standard: IPC/EAC J-STD-002, Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires
- Surface Mount Process Simulation Test (Preconditioning 16 hours ±30minutes dry bake)
- Operating Condition: Unpowered

8: Regulatory Compliance and Industry Certifications

This chapter describes the current certification status of the RC7110 and RC7120 (hereinafter collectively referred to as "RC71xx"). Certifications in other countries may be attained upon customer request—contact your Sierra Wireless account representative for details.

Additional testing and certification may be required for the host product with an embedded RC71xx module and are the responsibility of the OEM. Sierra Wireless offers professional services-based assistance to OEMs with the testing and certification process, if required.

8.1 Regulatory Compliance

The RC71xx module meets the requirements of the following regulatory bodies and regulations, where applicable:

- Federal Communications Commission (FCC) of the United States
- Innovation, Science and Economic Development Canada (ISED)
- Radio Equipment Directive (RED)
- The National Communications Commission (NCC) of Taiwan, Republic of China

8.1.1 Important Compliance Information for Canada and the United States

The RC7110 module has been granted modular approval for mobile applications under:

- FCC ID: N7NRC71A
- IC: 2417C-RC71A

Integrators may use the RC7110 module in their host products without additional FCC/ISED certification if they meet the following conditions. Otherwise, additional FCC/ISED approvals must be obtained.

1. The host product must use the RF trace design approved for the RC7110 module. The Gerber file of the trace can be obtained from Sierra Wireless upon request.
2. At least 20 cm separation distance between the antenna and the user's body must be maintained at all times.
3. To comply with FCC/ISED regulations limiting both maximum RF output power and human exposure to RF radiation, the maximum antenna gain including cable loss in a mobile-only exposure condition must not exceed the limits stipulated in Table 8-1.
4. The RC7110 may transmit simultaneously with other collocated radio transmitters within a host product, provided the following conditions are met:
   - Each collocated radio transmitter has been certified by FCC/ISED for mobile application.
   - At least 20 cm separation distance between the antennas of the collocated transmitters and the user's body must be maintained at all times.
   - The radiated power of a collocated transmitter must not exceed the EIRP limit stipulated in Table 8-1.

Table 8-1: Antenna Gain Specifications

Device	Operating Mode	Tx Freq Range (MHz)		Max Conducted Power (dBm)	Maximum Antenna Gain (dBi)	
					Standalone	Collocated
RC7110	LTE B2	1850	1910	24	9.0	6.4
	LTE B4	1710	1755	24	6.0	6.0
	LTE B8 (FCC only)	897.5	900.5	24	10.5	4.0
	LTE B12	699	716	24	6.6	3.5
	LTE B13	777	787	24	6.9	3.8
	LTE B66	1710	1780	24	6.0	6.0
Collocated transmitters				Maximum EIRP (dBm)		
	WLAN 2.4 GHz	2400	2500	31.0		
	WLAN 5 GHz	5150	5850	31.0		
	Bluetooth	2400	2500	20.0		

5. A label must be affixed to the outside of the host product into which the RC7110 is incorporated, with a statement similar to the following:
   - **This device contains FCC ID: N7NRC71A / IC: 2417C-RC71A**
6. A user manual with the host product must clearly indicate the operating requirements and conditions that must be observed to ensure compliance with current FCC/ISED RF exposure guidelines.

Note: Host product manufacturers are responsible for the overall compliance of the host products including, where applicable, all additional equipment authorization and testing not covered by the modular approval (e.g., unintentional radiator FCC Part 15 Subpart B requirements, ISED's Interference-Causing Equipment Standards, and RF exposure requirements for host products intended for use within 20 cm of the user's body.)

8.2 Industry Certifications

The RC71xx module complies with the mandatory requirements described in the following standards. The exact set of requirements supported is network operator-dependent.

Table 8-2: Standards Compliance

Technology	Standards
LTE	3GPP Release 14

The following industry certifications have been obtained, where applicable:
- GCF
- PTCRB

9: Pinout

The system interface of the Sierra Wireless RC71xx is through the LGA pattern on the bottom of the PCB.

Sierra Wireless RC71xx pins are divided into three functional categories:

- Core functions and associated pins — Cover all the mandatory features for M2M connectivity and will be available by default across all CF3 family of modules. These Core functions are always available and always at the same physical pin locations. A customer platform using only these functions and associated pins is guaranteed to be forward and/or backward compatible with the next generation of CF3 modules.
- Extension functions and associated pins — Bring additional capabilities to the customer. Whenever an Extension function is available on a module, it is always at the same pin location.
- Custom functions and associated pins — These are module-specific and make use of specific chipset functions and I/Os.

Warning: *Custom features should be used with caution as there is no guarantee that the custom functions available on a given module will be available on other CF3 modules.*

Pins marked as "Leave open" or "Reserved" should not be used or connected.

9.1 Pin Configuration

Figure 9-1 illustrates the pin configuration of the Sierra Wireless RC71xx module.

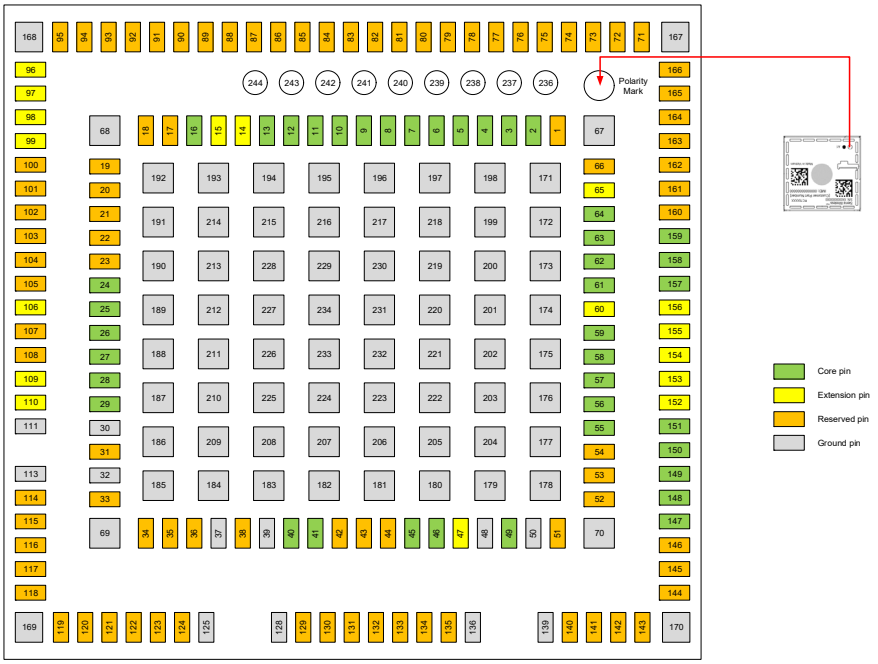


Figure 9-1: Pin Configuration (Top View, Through Module)

9.2 Pin Description

Table 9-1 on page 77 lists detailed information for the LGA pins.

Note: Pin numbers 112/126/127/137/138/235 do not appear in this table because there are no corresponding pads on the module's PCB.

Table 9-1: Pin Definitions

Pin	Signal Name	Group	I/O[a]	Voltage	Pull Type[b]	Active	If Unused	Function	Type
1	Reserved	No connection					See footnote[c]		Reserved
2	UART1_RI[d,e]	UART1	O	1.8V/3.3V[f]		L	Leave open	UART1 Ring indicator	Core
		Note: Do not install external pull-up on this pin, otherwise the module will not boot.							
3	UART1_RTS[d]	UART1	I	1.8V/3.3V[f]	PD	L	Leave open	UART1 Request to send	Core
4	UART1_CTS[d]	UART1	O	1.8V/3.3V[f]		L	Leave open	UART1 Clear to send	Core
5	UART1_TX[d]	UART1	I	1.8V/3.3V[f]	PD	L	Leave open	UART1 Transmit data	Core
6	UART1_RX[d]	UART1	O	1.8V/3.3V[f]			Leave open	UART1 Receive data	Core
7	UART1_DTR[d,g,h]	UART1	I	1.8V	PD	L	Leave open	UART1 Data terminal ready	Core
8	UART1_DCD[d,e]	UART1	O	1.8V/3.3V[f]		L	Leave open	UART1 Data carrier detect	Core
		Note: Do not install external pull-up on this pin, otherwise the module will not boot.							
9	UART1_DSR[d,e]	UART1	O	1.8V/3.3V[f]		L	Leave open	UART1 Data set ready	Core
		Note: Do not install external pull-up on this pin, otherwise the module will not boot.							
10	GPIO2[g,h,m]	GPIO	I/O	1.8V/3.3V[i]	PD		Leave open	General purpose I/O	Core
11	RESET_IN_N[j]	Control signal	I	1.8V	PU	L	Leave open	Input reset signal	Core
12	USB_D-	USB	I/O				Leave open	USB Data negative	Core
13	USB_D+	USB	I/O				Leave open	USB Data positive	Core
14–15	Reserved	No connection					See footnote[c]		Reserved

Table 9-1: Pin Definitions (Continued)

Pin	Signal Name	Group	I/O[a]	Voltage	Pull Type[b]	Active	If Unused	Function	Type
16	USB_VBUS	USB	I	5V or VBAT_BB			Optional connection ▪ If USB interface is required, connect to USB_VBUS ▪ If unavailable, connect to VBAT_BB ▪ Otherwise, leave open	▪ Indicate USB status ▪ Use as a trigger for booting the module	Core
17–23	Reserved	No connection					See footnote[c]		Reserved
24	ADC1	ADC	AI	0–1.2V			Leave open	Analog to digital conversion	Core
25	ADC0	ADC	AI	0–1.2V			Leave open	Analog to digital conversion	Core
26	UIM1_VCC	UIM1	Power Output	1.8V/3V			Mandatory connection	UIM1 Power supply	Core
27	UIM1_CLK	UIM1	O	1.8V/3V			Mandatory connection	UIM1 Clock	Core
28	UIM1_DATA	UIM1	I/O	1.8V/3V	PU		Mandatory connection	UIM1 Data	Core
29	UIM1_RESET_N	UIM1	O	1.8V/3V		L	Mandatory connection	UIM1 Reset	Core
30–39	Reserved	No connection					See footnote[c]		Reserved
40	GPIO7	GPIO	I/O	1.8V/3.3V[f]	PD		Leave open	General purpose I/O	Core
41	GPIO8	GPIO	I/O	1.8V/3.3V[f]	PD		Leave open	General purpose I/O	Core
42–44	Reserved	No connection					See footnote[c]		Reserved
45	VGPIO	Voltage reference	Power Output	1.8V/3.3V[f]			Leave open	GPIO voltage output	Core
46	GPIO6[k]	GPIO	I/O	1.8V/3.3V[f]	PD		Leave open	General purpose I/O	Core
	RESET_OUT_N	Control Signal	O	1.8V/3.3V[f]			Leave open	Reset output signal	Core
47	TP1 (Boot pin)	Control Signal	I	1.8V/3.3V[f]		L	Required test point for Sierra Wireless RMA debugging	Test point 1 ▪ 0 — Download mode ▪ Open — Normal mode	Extension
48	GND	Ground	0V	0V			Mandatory connection	Main antenna ground	Core
49	RF_MAIN	RF	AI, AO				Mandatory connection	Main RF antenna	Core

Table 9-1: Pin Definitions (Continued)

Pin	Signal Name	Group	I/O[a]	Voltage	Pull Type[b]	Active	If Unused	Function	Type
50	GND	Ground	0V	0V			Mandatory connection	Main antenna ground	Core
51–54	Reserved	No connection					See footnote[c]		Reserved
55	Reserved	No connection					See footnote[c]		Core
	UIM2_VCC	UIM2	Power Output	1.8V			Leave open	UIM2 Power	
56	Reserved	No connection					See footnote[c]		Core
	UIM2_DATA	UIM2	I/O	1.8V	PU		Leave open	UIM2	
57	Reserved	No connection					See footnote[c]		Core
	UIM2_RESET_N	UIM2	O	1.8V	PU		Leave	UIM2	
58	Reserved	No connection					See footnote[c]		Core
	UIM2_CLK	UIM2	O	1.8V			Leave open	UIM2 Clock	
59	POWER_ON_N	Control Signal	I	2V (floating)	PU	L	Mandatory connection	Power On control signal	Core
60	Reserved	No connection					See footnote[c]		Reserved
61	VBAT_RF	Power	Power Input	3.4V (min) 3.7V (typ) 4.3V (max)			Mandatory connection	RF power supply (see Power Supply Ratings)	Core
62	VBAT_RF	Power	Power Input	3.4V (min) 3.7V (typ) 4.3V (max)			Mandatory connection	RF power supply (see Power Supply Ratings)	Core
63	VBAT_BB	Power	Power Input	3.4V (min) 3.7V (typ) 4.3V (max)			Mandatory connection	Baseband power supply (see Power Supply Ratings)	Core
64	UIM1_DET[g,h,j]	UIM1	I	1.8V	PU	H	Mandatory connection	Detect UIM1 insertion/removal. Note — Pin must be open to detect the UIM, or grounded if no UIM is present.	Core

Table 9-1: Pin Definitions (Continued)

Pin	Signal Name	Group	I/O[a]	Voltage	Pull Type[b]	Active	If Unused	Function	Type
65	UIM2_DET[g,h,j]	UIM2	I	1.8V	PU	H	Leave open	Detect UIM2 insertion/removal Note — Pin must be open to detect the UIM, or grounded if no UIM is present.	Extension
	GPIO4[i,j]	GPIO	I	1.8V	PU		Leave open	Input only	Extension
66	Reserved	No connection					See footnote[c]		Reserved
67–70	GND	Ground	0V	0V			Mandatory connection	Ground	Core
71–95	Reserved	No connection					See footnote[c]		Reserved
96	UART2_TX[d]	UART2	I	1.8V/3.3V[f]	PD	L	Leave open	UART2 Transmit data	Extension
97	UART2_RX[d]	UART2	O	1.8V/3.3V[f]	PD	L	Leave open	UART2 Receive data	Extension
98	UART2_RTS[d]	UART2	I	1.8V/3.3V[f]	PD		Leave open	UART2 Request To Send	Extension
99	UART2_CTS[d]	UART2	O	1.8V/3.3V[f]			Leave open	UART2 Clear To Send	Extension
100–105	Reserved	No connection					See footnote[c]		Reserved
106	WWAN_LED_N	Indication	O	1.8V/3.3V[f]		L	Leave open	LED driver control	Extension
107–108	Reserved	No connection					See footnote[c]		Reserved
109	GPIO42[g,h,j]	GPIO	I	1.8V	PU		Leave open	Input only	Extension
110	WAKE_ON_WWAN	Indication	O	1.8V/3.3V[f]		H	Leave open	Driven high to wake the host when specific events occur.	Extension
111	Reserved	No connection					See footnote[c]		Reserved
113	Reserved	No connection					See footnote[c]		Reserved
114–124	Reserved	No connection					See footnote[c]		Reserved
125	Reserved	No connection					See footnote[c]		Reserved
128	Reserved	No connection					See footnote[c]		Reserved
129–135	Reserved	No connection					See footnote[c]		Reserved
136	GND	Ground	0V	0V			Mandatory connection	Main antenna ground	Core

Table 9-1: Pin Definitions (Continued)

Pin	Signal Name	Group	I/O[a]	Voltage	Pull Type[b]	Active	If Unused	Function	Type
139	GND	Ground	0V	0V			Mandatory connection	Main antenna ground	Core
140–144	Reserved	No connection					See footnote[c]		Reserved
145	IO_VOL_SEL	GPIO Power domain control						Voltage leel selection: ▪ Open — VGPIO = 1.8 V ▪ 0 (Ground) — VGPIO = 3.3 V	Extension
146	Reserved	No connection					See footnote[c]		Reserved
147	GPIO21[g,h,m]	GPIO	I/O	1.8V / 3.3V[i]	PD		Leave open	General purpose I/O	Core
148	GPIO22	GPIO	I/O	1.8V / 3.3V[f]	PD		Leave open	General purpose I/O	Core
149	GPIO23	GPIO	I/O	1.8V / 3.3V[f]	PD		Leave open	General purpose I/O	Core
150	GPIO24	GPIO	I/O	1.8V / 3.3V[f]	PD		Leave open	General purpose I/O	Core
151	W_DISABLE_N	Control Signal	I	1.8V / 3.3V[f]	PU	L	Leave open	Wireless disable (main RF radio)	Core
152	SAFE_PWR_REMOVE	Indication	O	1.8V / 3.3V[f]		H	Leave open	Indicate to host that Main DC power can be removed	Extension
153	ANT_CNTL0	Antenna control	O	1.8V			Leave open	Antenna control	Extension
154	ANT_CNTL1	Antenna control	O	1.8V			Leave open	Antenna control	Extension
155	GPIO30[m]	GPIO	I/O	1.8V / 3.3V[f]	PD		Leave open	General purpose I/O	Extension
156	GPIO31[m]	GPIO	I/O	1.8V / 3.3V[f]	PD		Leave open	General purpose I/O	Extension
157	VBAT_RF	Power	Power Input	3.4V (min) 3.7V (typ) 4.3V (max)			Optional connection	RF power supply (see Power Supply Ratings)	Core
158	VBAT_BB	Power	Power Input	3.4V (min) 3.7V (typ) 4.3V (max)			Optional connection	Baseband power supply (see Power Supply Ratings)	Core
159	GPIO25	GPIO	I/O	1.8V / 3.3V[f]	PD		Leave open	General purpose I/O	Core
160–166	Reserved	No connection					See footnote[c]		Reserved

Table 9-1: Pin Definitions (Continued)

Pin	Signal Name	Group	I/O[a]	Voltage	Pull Type[b]	Active	If Unused	Function	Type
167–234	GND	Ground	0V	0V			Mandatory connection	Ground	Core
236–244	Reserved	No connection					See footnote[c]		Reserved

a. Signal direction with respect to the module.
b. NP — No Pull; PD — Pull Down; PU — Pull Up (in default/active normal mode)
c. Pins are connected internally, but are reserved for future use. Leave them unconnected to ensure compatibility with other Sierra Wireless CF3 modules.
d. (UART signals only) Signals are named with respect to the host device. For example, UART1_RX is the signal used by the host to receive data from the module.
e. Do not install external pull-up on this pin, otherwise the module will not boot.
f. Pin supports 1.8 V or 3.3 V depending on the state of pin 145 (IO_VOL_SEL).
When IO_VOL_SEL is:
   - Floating — Indicated pins support 1.8V.
   - Connected to ground — Indicated pins support 3.3V.
g. Pin is 'wakeable'. Can be used to trigger the module to wake up from Sleep mode. For details, see Table 3-8: Modem Wakeup Sources (Hardware).
h. Refer to Table 3-25 for GPIO2, GPIO21, GPIO42, UART1_DTR, UIM1_DET, and UIM2_DET/GPIO4 pin voltage requirement details.
i. GPIO2 and GPIO21 support:
   - 1.8 V in their default configuration as wakeup sources. Refer to Table 3-25 for pin voltage requirement details.
   - 1.8 V or 3.3 V as described in footnote 'f', when configured for GPIO mode using **AT+WIOCFG**.
j. Do not install external pull-ups on GPIO42, RESET_IN_N, UIM1_DET, UIM2_DET/GPIO4.
k. Refer to GPIO6 for functional details.
l. Refer to GPIO4 for functional details.
m. This pin is available for use when configured using **AT+WIOCFG**.

Table 9-2: RF Pin Information

Signal name	Pin #	Description
RF_MAIN	49	Main RF port (input/output)

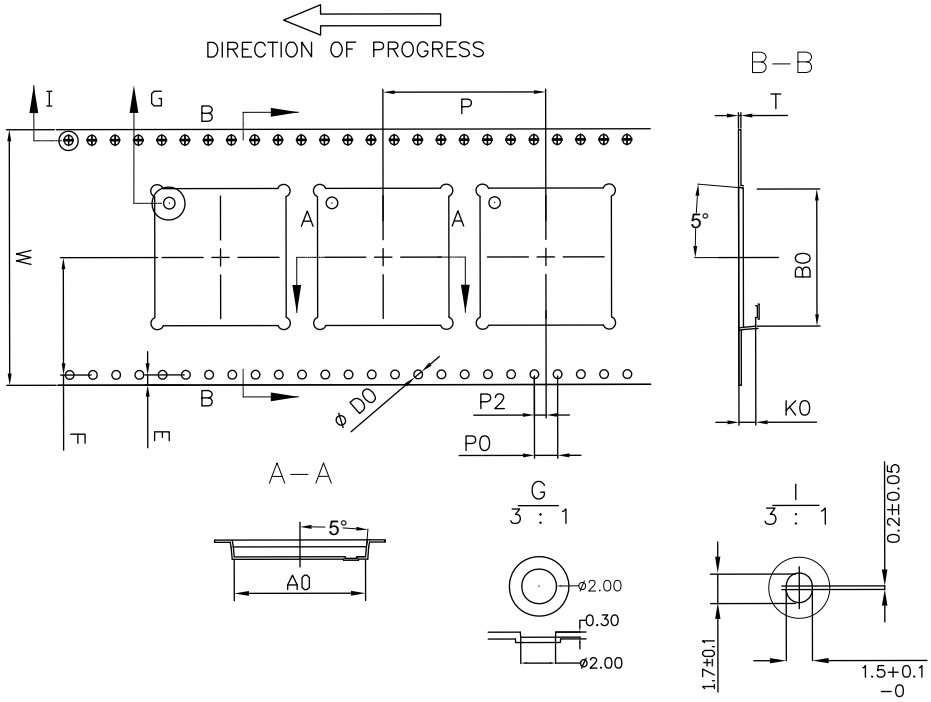
Table 9-3: Supply Pin Information

Signal name	Pin #	Description
VBAT_RF	61, 62, 157	RF power supply
VBAT_BB	63, 158	Baseband power supply
USB_VBUS	16	Connected to USB_VBUS (5V) or (if unavailable) VBAT_BB. Used only for detecting USB status and is not intended as a power supply pin for the module.

10: Packaging

Sierra Wireless RC71xx modules are delivered in tape and reel format (Figure 10-1, Figure 10-2).

Quantity per tape and reel: 500 modules



P	P0	P2	W	Ø D0	E	F	A0	B0	K0	T
28 mm	4.0 mm	2.0 mm	44.0 mm	1.5 mm	1.75 mm	20.2 mm	22.6 mm	23.6 mm	2.9 mm	0.4 mm

Figure 10-1: Tape

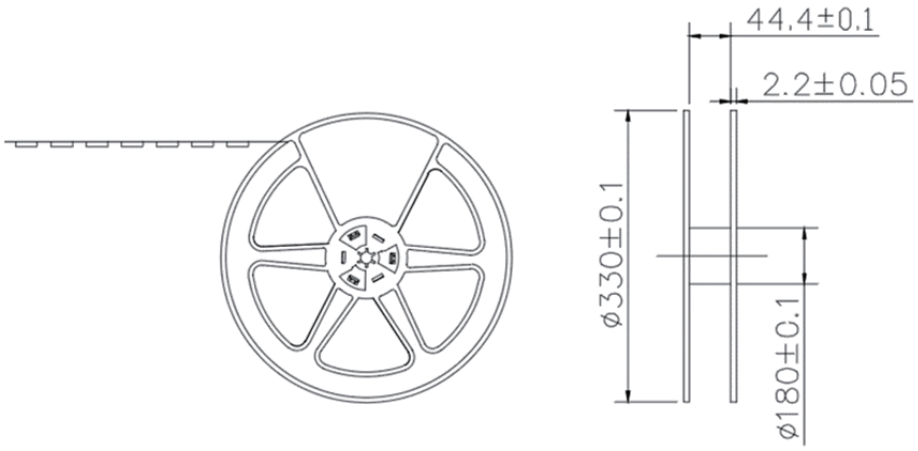


Figure 10-2: Reel

Reels are packaged for delivery by Sierra Wireless using the following process:

1. Reel preparation (Figure 10-3):
   a. An ESD-strap (SP1) is applied to the outside band of the reel (T2).
   b. A moisture-sensitive label (see callout) and a manufacturing box label (L2) are placed on the reel.
   c. Three dessicant packets (DS1) and a humidity indicator card (H1) are centered on the top of the reel.
   d. Another manufacturing box label (L2) is placed on the vacuum bag (BG1), and all items are sealed inside the vacuum bag.
   e. The vacuum bag (BG1) is folded.

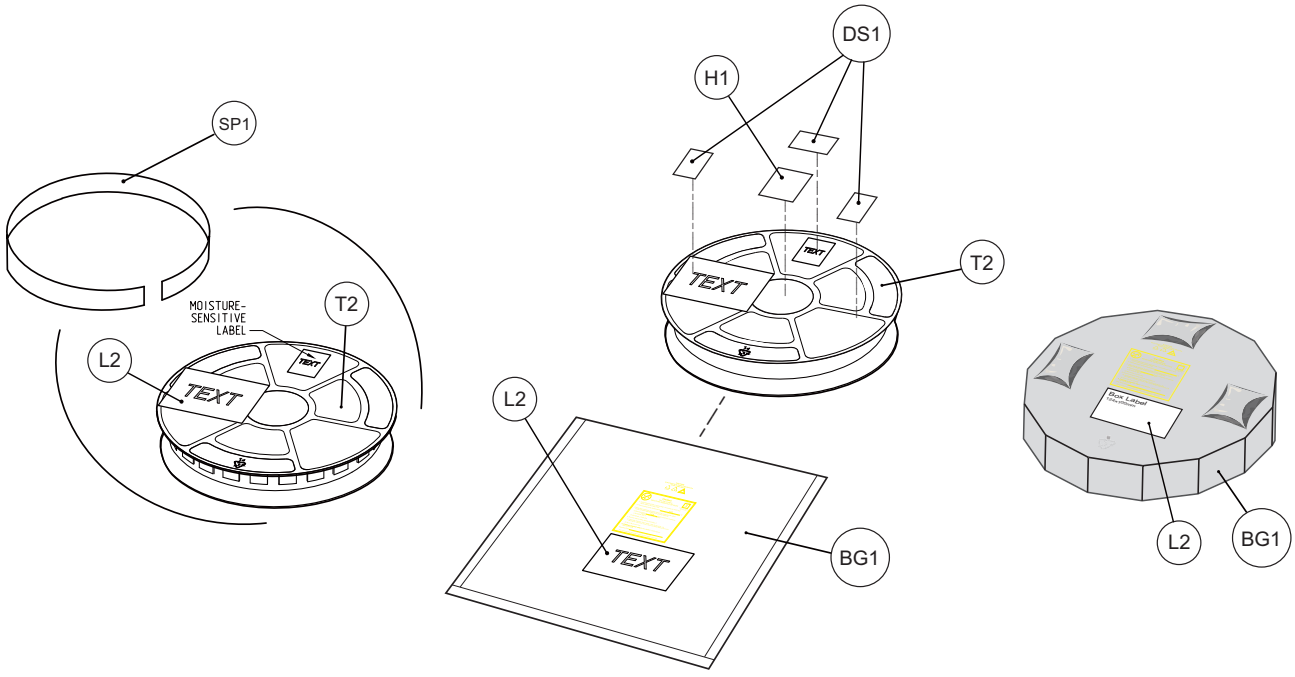


Figure 10-3: Reel Preparation

2. Manufacturing box preparation (Figure 10-4):
   a. The vacuum bag (BG1) is placed in a manufacturing box (B2) with an ESD foam pad on the top and and ESD foam gasket on the bottom.
   b. The box is sealed with security tape (P1).
   c. A moisture-sensitive identification (MSID) label and manufacturing box label (L2) are placed on the top of the box in the bottom-right corner.

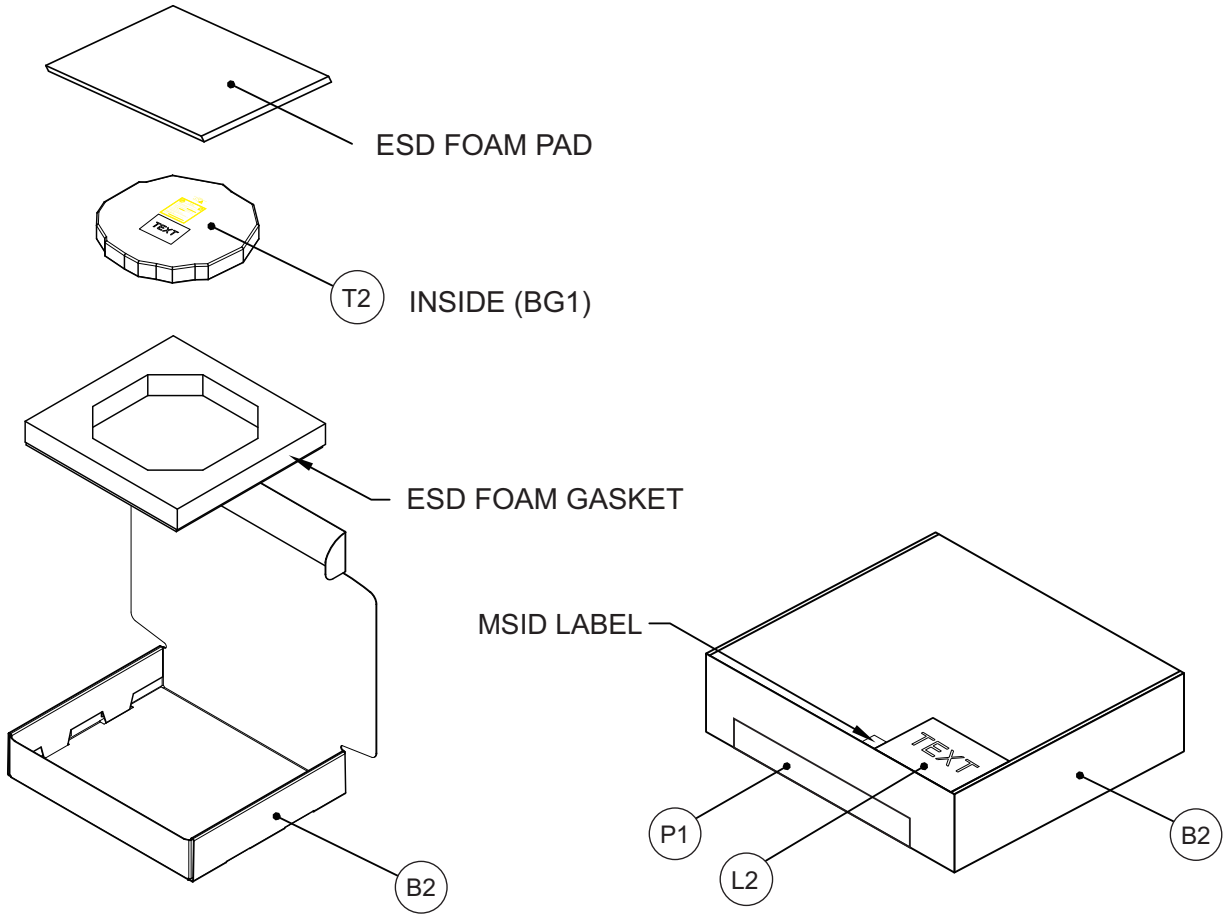


Figure 10-4: Manufacturing Box Preparation

3. Shipping carton preparation (Figure 10-5):
   - **a.** The manufacturing box (B2) is placed into a shipping carton (B4).
   - **b.** The carton is sealed with tape (P2) in an 'H'-pattern covering the seams on the top of the carton.
   - **c.** A carton label (L3) is placed on the top of the carton in the bottom-right corner.
   - **d.** The shipping carton (B4) is wrapped with ≥ 3 layers of PE film.

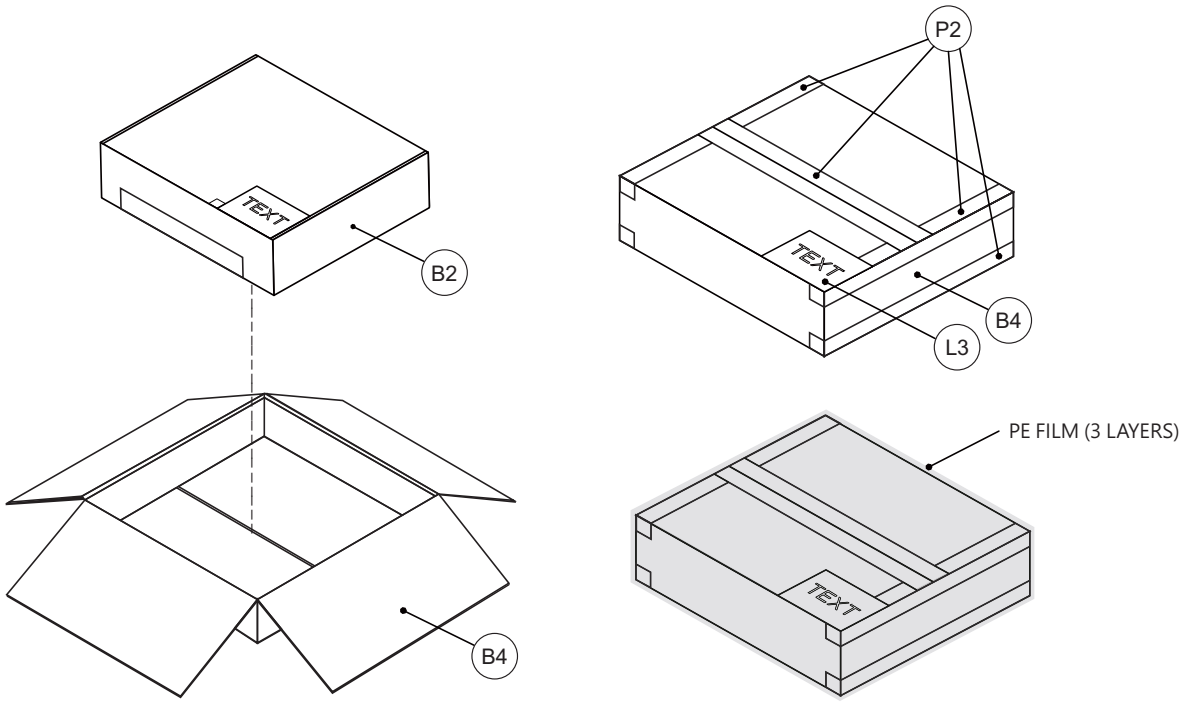


Figure 10-5: Shipping Carton Preparation

11: Testing

11.1 Certification Testing

Note: Typically, certification testing of your host device with the integrated module is required one time only.

The Sierra Wireless RC71xx module has been certified as described in Regulatory Compliance and Industry Certifications.

When you produce a host device with a Sierra Wireless embedded module, you must obtain certifications for the final product from appropriate regulatory bodies in the jurisdictions where it will be distributed.

The following are *some* of the regulatory bodies from which you may require certification — it is your responsibility to make sure that you obtain all necessary certifications for your product from these or other groups:

- FCC (Federal Communications Commission — www.fcc.gov)
- GCF (Global Certification Forum — www.globalcertificationforum.org) outside of North America
- PTCRB (PCS Type Certification Review Board — www.ptcrb.com) in North America

11.2 Production Testing

Note: Production testing typically continues for the life of the product.

Production testing ensures that, for each assembled device, the module is installed correctly (I/O signals are passed between the host and module), and the antenna is connected and performing to specifications (RF tests).

Typical items to test include:

- Host connectivity
- Baseband (host/module connectors)
- RF assembly (Tx and/or Rx, as appropriate)
- Network availability
- Host/device configuration issues

*Note: The number and types of tests to perform are **your** decision — the tests listed in this section are guidelines only. Make sure that the tests you perform exercise functionality to the degree that **your** situation requires.*

Use an appropriate test station and use AT commands to control the integrated module.

Note: Your test location must be protected from ESD to avoid interference with the module and antenna(s), assuming that your test computer is in a disassembled state.
Also, consider using an RF shielding box — local government regulations may prohibit unauthorized transmissions.

11.3 Functional Production Test

This section presents a suggested procedure for performing a basic manual functional test on a laboratory bench using a Sierra Wireless RC71xx module and a hardware development kit. When you have become familiar with the testing method, use it to develop your own automated production testing procedures.

11.3.1 Suggested Production Tests

Consider the following tests when you design your production test procedures for devices with the module installed.

- Visual check of the module's connectors and RF assemblies
- Module is operational
- USB connection is functional
- LED is functional
- Power on/off
- Firmware revision check
- Rx tests
- Tx test

11.3.2 Production Test Procedure

The following is a suggested test plan — you must decide which tests are appropriate for your product. You may wish to add additional tests that more fully exercise the capabilities of your product.

Using an appropriate test station, and referring to the appropriate AT command references:

1. Visually inspect the module for obvious defects (such as tainted or damaged shields) before installing it in the test station.
2. Ensure that the module is powered off (no voltage on VBAT_BB/VBAT_RF) before beginning your tests.
3. Provide power to the module (voltage on VBAT_BB/VBAT_RF).

   Test POWER_ON_N — Turn on the module by driving POWER_ON_N low, as shown in Figure 4-1.
4. Test USB functionality:
   a. Check for USB enumeration — open Windows Device Manager and confirm that three "USB Serial Device (COM###) ports are listed:

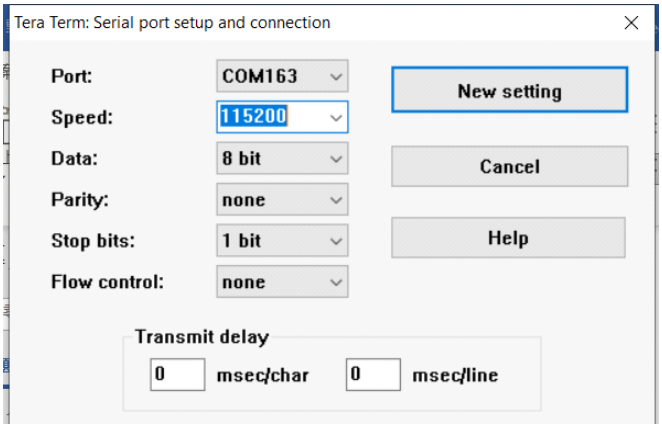
   b. Make sure your module is connected and running, and then establish contact with the module — Use a terminal emulation/communications program such as TeraTerm or PuTTY to connect over the device handle for AT commands.

For example, using TeraTerm (available from the TeraTerm open source site github.com/TeraTermProject/teraterm/releases):

i. Start TeraTerm.

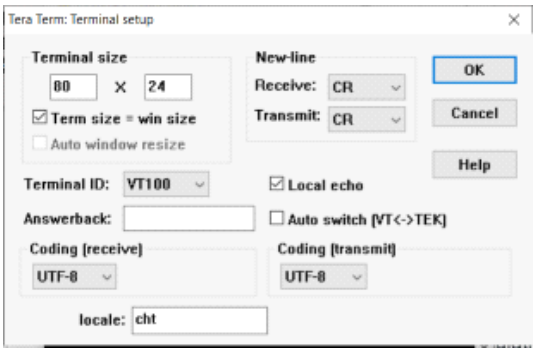
ii. Select File→New Connection→Serial [Port: USB Serial Device (COMn)]

iii. Select Setup→Serial port and use the following settings: Speed=115200; Data= 8 bit; Parity=none; Stop bits=1 bit]; Flow Control=none:



iv. Click New setting.

v. Select Setup→Terminal and use the following setting: Local echo=V. (This step is optional, to echo your commands on screen.)



vi. Display the firmware version:

```
ATI
```

If you can enter the command and view a response, the USB connection is working.

5. Unlock the extended AT command set:

```
AT!ENTERCND="<key>"  ← <key> — Unlock key code
```

6. Test the LED — Visually confirm that the LED turns on and off:

```
AT!LEDPATTERN=1  ← LED on
AT!LEDPATTERN=0  ← LED off
AT!LEDPATTERN=2,50,200  ← PWM <mode>, <pwm_duration>,<pwm_cycle>
```

7. Put the module in diagnostic/factory test mode:

```
AT!DAFTMACT
```

8. Make sure the test SIM is working correctly. For example, the commands **AT+CPIN** and **AT+CIMI** can be used to test the SIM.

9. Test RF transmission, if desired — see LTE RF Transmission Path Test on page 90.
10. Test RF reception, if desired — see LTE RF Receive Path Test on page 91.
11. Remove power from the module.

11.4 LTE RF Transmission Path Test

Important: *As of the publication date of this document, the test procedure described is to be considered preliminary, pending implementation of some commands in a future firmware upgrade.*

Note: This procedure segment is performed in step 9 of the Production Test Procedure on page 88.

The suggested test procedure that follows uses the parameters in the following tables.

Table 11-1: Test Settings — RC7110 LTE Transmission Path

Band		Frequency (MHz)	Channel[a]
1900 MHz	B2	1880.0	18900
1700 MHz	B4	1732.5	20175
900 MHz	B8	897.5	21625
700 MHz	B12	707.5	23095
700 MHz	B13	782.0	23230
1700 MHz	B66	1745.0	132322

a. Channel value is used by the `+WMTXPOWER` command (+WMTXPOWER uses uplink (Tx) channel at the center of the corresponding band.)

Table 11-2: Test Settings — RC7120 LTE Transmission Path

Band		Frequency (MHz)	Channel[a]
2100 MHz	B1	1950.0	18300
1800 MHz	B3	1747.5	19575
2600 MHz	B7	2535.0	21100
900 MHz	B8	897.5	21625
800 MHz	B20	847.0	24300
700 MHz	B28	725.5	27435

a. Channel value is used by the `+WMTXPOWER` command (+WMTXPOWER uses uplink (Tx) channel at the center of the corresponding band.)

Note: This procedure describes steps using a Giga-tronics Power Meter.

To test the DUT's transmitter path:

1. Set up the power meter:
   a. Make sure the meter has been given sufficient time to warm up, if necessary, to enable it to take accurate measurements.
   b. Zero-calibrate the meter.
   c. Enable MAP mode.
2. Prepare the DUT using the following AT commands (adjusting the band, channel, bandwidth, and power level as necessary):
   a. Unlock the extended AT command set:
      ```
      AT!ENTERCND="<key>"  ← <key> — Unlock key code
      ```
   b. Put the module in diagnostic/factory test mode:
      ```
      AT!DAFTMACT
      ```
   c. Set the frequency band (e.g., LTE B1) and other parameters:
      ```
      AT+WMTXPOWER=1,1,18300,2300,0,0
      ```
      For appropriate parameter values (including bands and channels), see Table 11-1 / Table 11-2. For more details, refer to *[1] RC71xx AT Command Reference (Doc# 41114675)*.
   d. Take the measurement.
   e. Repeat step c with different power levels if desired.
   f. Turn off the transmitter:
      ```
      AT!WMTXPOWER=0
      ```
3. Test limits — Run ten or more good DUTs through this test procedure to obtain a nominal output power value.
   - Apply a tolerance of 5–6 dB to each measurement (assuming a good setup design).
   - Monitor these limits during mass-production ramp-up to determine if further adjustments are needed.

Note: The module has a nominal output power of +23 dBm +1/-2 dB in LTE mode. However, the value measured by the power meter is significantly influenced (beyond the stated +1/-2 dB output power tolerance) by the test setup (host RF cabling loss, antenna efficiency and pattern, test antenna efficiency and pattern, and choice of shield box).

Note: When doing the same test over the air in an RF chamber, values are likely to be significantly lower.

11.5 LTE RF Receive Path Test

Note: This procedure segment is performed in step 10 of the Production Test Procedure on page 88.

The suggested test procedure that follows uses the parameters in the following tables.

Table 11-3: Test Settings — RC7110 LTE Receive Path

Band		Frequency[a] (MHz)	Channel[b]
1900 MHz	B2	1962.0	900
1700 MHz	B4	2134.5	2175
900 MHz	B8	944.5	3625
700 MHz	B12	739.5	5095
700 MHz	B13	753.0	5230
1700 MHz	B66	2157.0	66886

a. Receive frequencies shown are 2 MHz offset from center.
b. Channel value is used by the `+WMTXPOWER` command (+WMTXPOWER uses the downlink (Rx) channel at the center of the corresponding band, for Rx testing.)

Table 11-4: Test Settings — RC7120 LTE Receive Path

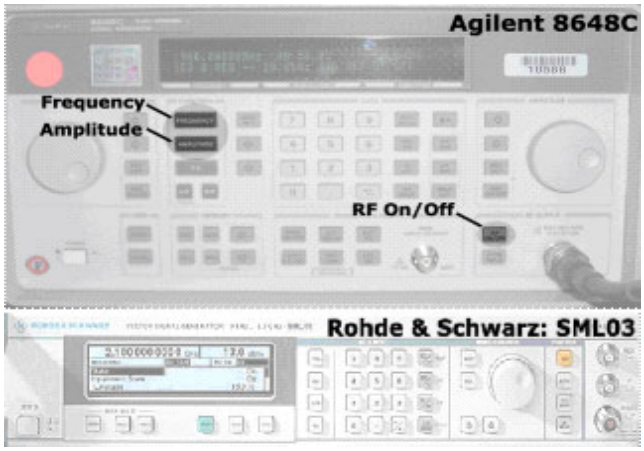
Band		Frequency[a] (MHz)	Channel[b]
2100 MHz	B1	2142.0	300
1800 MHz	B3	1844.5	1575
2600 MHz	B7	2657.0	3100
900 MHz	B8	944.5	3625
800 MHz	B20	808.0	6300
700 MHz	B28	782.5	9435

a. Receive frequencies shown are 2 MHz offset from center.
b. Channel value is used by the `+WMTXPOWER` command (+WMTXPOWER uses the downlink (Rx) channel at the center of the corresponding band, for Rx testing.)

Note: This procedure describes steps using the Agilent 8648C signal generator — the Rohde & Schwarz SML03 is shown for reference only

To test the DUT's receive path:

1. Set up the signal generator:



   a. Set the amplitude to -70 dBm.
   b. Set the frequency for the band being tested. See Table 11-3/Table 11-4 for frequency values.

2. Set up the DUT:
   a. Unlock the extended AT command set:
      `AT!ENTERCND="<key>"` ← *<key> — Unlock key code*
   b. Put the module in diagnostic/factory test mode:
      `AT!DAFTMACT`
   c. Set the frequency band and DL channel:
      `AT+WMRXPOWER=1,1,300`

      For appropriate parameter values, see Table 11-3/Table 11-4. For more details, refer to *[1] RC71xx AT Command Reference (Doc# 41114675).*

3. Test limits — Run ten or more good DUTs through this test procedure to obtain a nominal received power value.
   - Apply a tolerance of 5–6 dB to each measurement (assuming a good setup design).
   - Make sure the measurement is made at a high enough level that it is not influenced by DUT-generated and ambient noise.
   - The Signal Generator power level can be adjusted and new limits found if the radiated test needs greater signal strength.
   - Monitor these limits during mass-production ramp-up to determine if further adjustments are needed.

Note: The value measured from the DUT is significantly influenced by the test setup and DUT design (host RF cabling loss, antenna efficiency and pattern, test antenna efficiency and pattern, and choice of shield box)

A: References

Sierra Wireless documents are available from source.sierrawireless.com, or on request (subject to license agreements or NDAs) from your Sierra Wireless representative.

A.1 Sierra Wireless Documents

Sierra Wireless Documents on the Source

The following documents are available from source.sierrawireless.com

[1] RC71xx AT Command Reference (Doc# 41114675)

[2] RC71xx Customer Process Guidelines (Doc# 41114682)

[3] RC71xx Linux Host Tools User Guide (Doc# 41114711)

[4] RC71xx Windows Host Tools User Guide (Doc# 41114805)

A.2 Industry / Other Documents

The following referenced document(s) are not provided by Sierra Wireless:

[5] Inter-Chip USB Supplement to the USB 2.0 Specification Revision 1.0

B: Abbreviations

Table B-1: Abbreviations and Definitions

Abbreviation or Term	Definition
3GPP	3rd Generation Partnership Project
ADC	Analog to Digital Converter
AP	Application Processor
API	Application Programming Interface
ASMB	AP SRAM Block
AT	Attention (prefix for modem commands)
BER	Bit Error Rate — A measure of receive sensitivity
BLER	Block Error Rate
CF3	Common Flexible Form Factor
CLK	Clock
CMOS	Complementary Metal Oxide Semiconductor
CP	Communication Processor
CPU	Central Processing Unit
CTS	Clear To Send
dB	Decibel = 10 x $\log_{10}$ (P1 / P2) *P1 is calculated power; P2 is reference power* Decibel = 20 x $\log_{10}$ (V1 / V2) *V1 is calculated voltage, V2 is reference voltage*
dBm	A logarithmic (base 10) measure of relative power (dB for decibels); relative to milliwatts (m). A dBm value will be 30 units (1000 times) larger (less negative) than a dBW value, because of the difference in scale (milliwatts vs. watts).
DC	Direct Current
DCD	Data Carrier Detect
DL	Downlink (network to mobile)
DRX	Discontinuous Reception
DSR	Data Set Ready
DSSS	Dual SIM Single Standby
DTR	Data Terminal Ready
eDRX	Extended Discontinuous Reception
EIRP	Effective (or Equivalent) Isotropic Radiated Power
EMC	Electromagnetic Compatibility

Table B-1: Abbreviations and Definitions (Continued)

Abbreviation or Term	Definition
ERP	Effective Radiated Power
ESD	Electrostatic Discharges
eSIM	Embedded SIM
FCC	Federal Communications Commission The U.S. federal agency that is responsible for interstate and foreign communications. The FCC regulates commercial and private radio spectrum management, sets rates for communications services, determines standards for equipment, and controls broadcast licensing. Consult www.fcc.gov.
FDD	Frequency Division Duplex
firmware	Software stored in ROM or EEPROM; essential programs that remain even when the system is turned off. Firmware is easier to change than hardware but more permanent than software stored on disk.
GND	Ground
GPIO	General Purpose Input Output
High-Z	High impedance
Host	The device into which an embedded module is integrated
Hz	Hertz = 1 cycle/second
I/O	Input/Output
IC	Industry Canada
I-eDRX	Idle mode eDRX
IMS	IP Multimedia Subsystem — Architectural framework for delivering IP multimedia services.
inrush current	Peak current drawn when a device is connected or powered on
IOT	Interoperability Testing
IS	Interim Standard. After receiving industry consensus, the TIA forwards the standard to ANSI for approval.
ISIM	IMS Subscriber Identity Module.
LED	Light Emitting Diode. A semiconductor diode that emits visible or infrared light.
LGA	Land Grid Array
LTE	Long Term Evolution—a high-performance air interface for cellular mobile communication systems.
MAX	Maximum
MHz	Megahertz = 10^6 Hz
MIC	Microphone
MIN	Minimum

Table B-1: Abbreviations and Definitions (Continued)

Abbreviation or Term	Definition
MO	Mobile Originated
MT	Mobile Terminated
N/A	Not Applicable
NVM	Non-volatile Memory
OEM	Original Equipment Manufacturer—a company that manufactures a product and sells it to a reseller.
packet	A short, fixed-length block of data, including a header, that is transmitted as a unit in a communications network.
PC	Personal Computer
PCB	Printed Circuit Board
PCS	Personal Communication System A cellular communication infrastructure that uses the 1.9 GHz radio spectrum.
PFM	Power Frequency Modulation
PSM	Power Saving Mode
PTCRB	PCS Type Certification Review Board
PWM	Pulse Width Modulation
QPSK	Quadrature Phase-Shift Keying
RAM	Random Access Memory
RAT	Radio Access Technology
RF	Radio Frequency
RI	Ring Indicator
RSE	Radiated Spurious Emissions
RST	Reset
RTC	Real Time Clock
RTS	Request To Send
RX	Receive
SED	Smart Error Detection
Sensitivity (Audio)	Measure of lowest power signal that the receiver can measure.
Sensitivity (RF)	Measure of lowest power signal at the receiver input that can provide a prescribed BER/BLER/SNR value at the receiver output.
SIM	Subscriber Identity Module.
SKU	Stock Keeping Unit—identifies an inventory item: a unique code, consisting of numbers or letters and numbers, assigned to a product by a retailer for purposes of identification and inventory control.
SMS	Short Message Service

Table B-1: Abbreviations and Definitions (Continued)

Abbreviation or Term	Definition
SNR	Signal-to-Noise Ratio
SRAM	Static Random Access Memory
TBC	To Be Confirmed
TBD	To Be Determined
TIA/EIA	Telecommunications Industry Association / Electronics Industry Association. A standards setting trade organization, whose members provide communications and information technology products, systems, distribution services and professional services in the United States and around the world. Consult www.tiaonline.org.
TIS	Total Isotropic Sensitivity
TP	Test Point
TX	Transmit
TYP	Typical
UART	Universal Asynchronous Receiver-Transmitter
UE	User Equipment
UICC	Universal Integrated Circuit Card
UIM	User Identity Module. Generic term used in this document to refer to UICC, where the application on the UICC (USIM, ISIM, CSIM, etc.) varies depending on the provider of the card.
UL	Uplink (mobile to network)
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module (UMTS)
VBATT	VBATT is a virtual signal that represents both VBAT_BB and VBAT_RF
VBAT_BB	Baseband power supply
VBAT_RF	RF power supply
VCC	Supply voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access (also referred to as UMTS)
WWAN	Wireless Wide Area Network